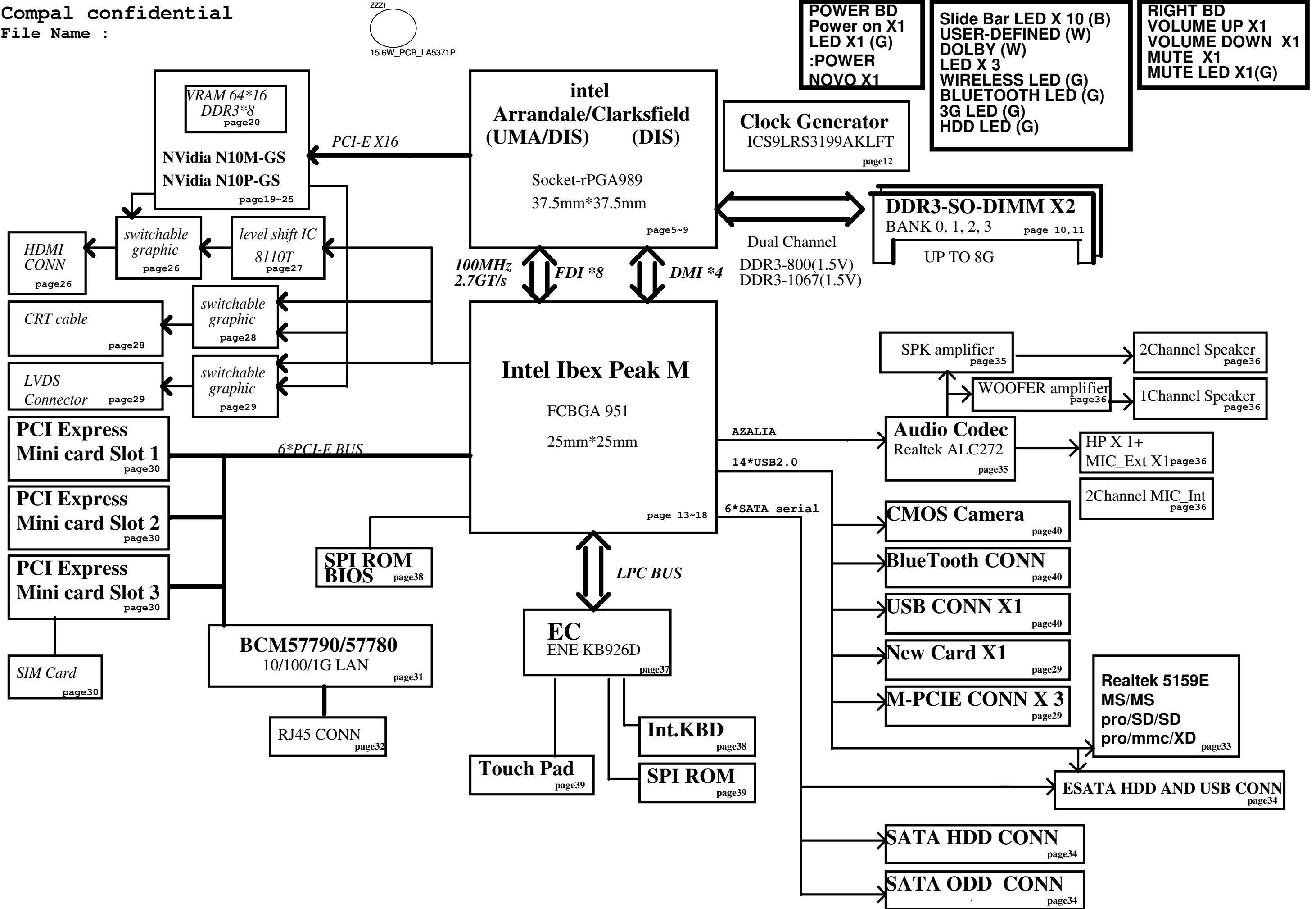


Compal Confidential
Schematics Document
Arrandale/Clarksville
with Intel IBEX PEAK-M core logic
NIWBA
REV: 0.1

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				Tuesday, March 24, 2009	0.1
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				2	52

DDR3 Voltage Rails

<div>power plane</div> <div>State</div>	+B	+5VALW +3VALW	+1.5V	<div>+5VS</div> <div>+3VS</div> <div>+1.5VS</div> <div>+VCCP</div> <div>+CPU_CORE</div> <div>+VGA_CORE</div> <div>+1.8VS</div> <div>+0.75VS</div> <div>+1.05VS</div>
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

@ FUNCTION

EVT		NON-USE	
45@	(45 BOM)		
GIGA@	(GIGA LAN)	100@	(100 LAN)
NO TVSW@	(NON TV POWER SW)	TVSW@	(TV POWER SW)
ARRAY@	(ARRAY MIC)	MONO@	(MONO MIC)
S512@	FOR X76 BOM		
H512@	FOR X76 BOM		
S1024@	FOR X76 BOM		
H1024@	FOR X76 BOM		
X76@	(X76 BOM)		
M1@	(DDR M1 MODE)		
3G@	(3G MODE)		
10M@	FOR 10M CHIP		
10P@	FOR 10P CHIP		
UMA@	FOR Auberndale		
DIS@	FOR Auberndale/Clarksfield		
VGA@	FOR NVIDIA PART		

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1 SMB_EC_DA1	KB926 +3VALW	X	V +3VALW	X	X	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926 +3VALW	X	X	X	X	X	X	X	X	X	X	V +3VALW
SMBCLK SMBDATA	PCH +3VALW	V +3VALW	X	X	V +3VS	V +3VS	X	X	X	X	V +3VS	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	X	X	V +3VALW	X	X	X	V +3VS	X	V +3VS	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

PCIE PORT LIST

PORT	DEVICE
1	NEW CARD
2	WLAN
3	LAN
4	3G
5	
6	TV TUNNER
7	
8	

USB PORT LIST

PORT	DEVICE
0	LEFT SIDE
1	RIGHT SIDE
2	CMOS
3	
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	TV TUNNER
10	NEW CARD
11	BT
12	
13	3G

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VGA and DDR3 Voltage Rails (N10x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	MEM_VID orPower supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP Link E
GPIO16	OUT	-	Programmable Fan Control
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	Hot plug detect for IFP Link D
GPIO20	IN	-	
GPIO21	IN	-	Hot plug detect for IFP link F
GPIO22	IN	-	SLI swap ready signal
GPIO23	I/O		

GPIO6	GPIO5	N10M-GS	N10P-GS
GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	1	0.9V	0, 10

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

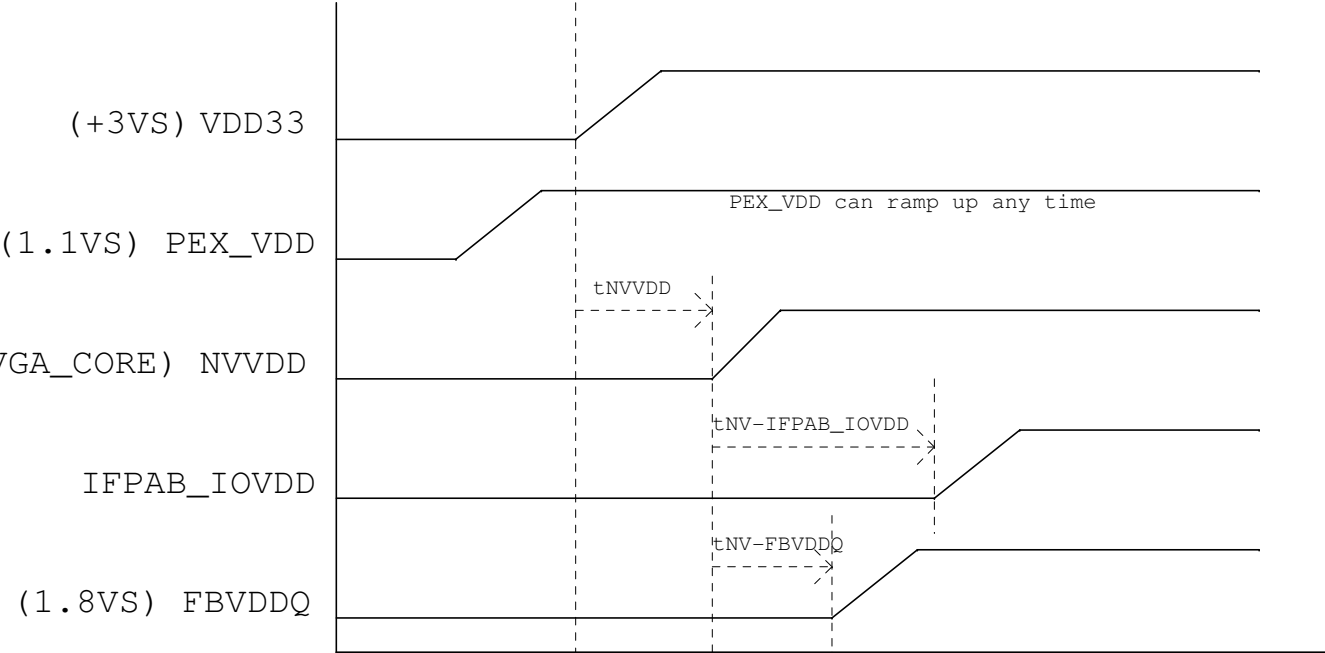
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK (MHz)	NVVDD			FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)		(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10P-GS 128bit 1024MB DDR3	21.07	6.67	TBD	TBD	18.25	17.34	2.06	3.09	4.09	6.14	850	0.89	75	0.14	63	0.07	55	0.18
N10P-GE 128bit 1024MB DDR3	20.97	6.73	TBD	TBD	19.17	17.25	2.03	3.05	4.09	6.14	840	0.88	75	0.14	63	0.07	55	0.18
N10P-LP 128bit 1024MB DDR3	15.48	6.44	TBD	TBD	13.95	11.86	1.90	2.85	3.99	5.99	810	0.85	75	0.14	63	0.07	55	0.18

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

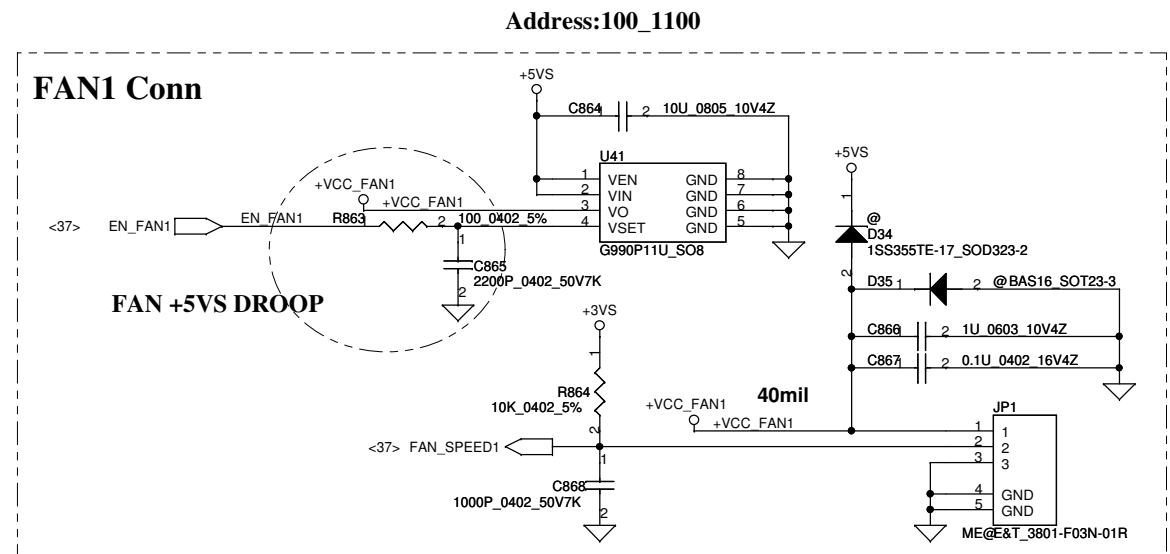
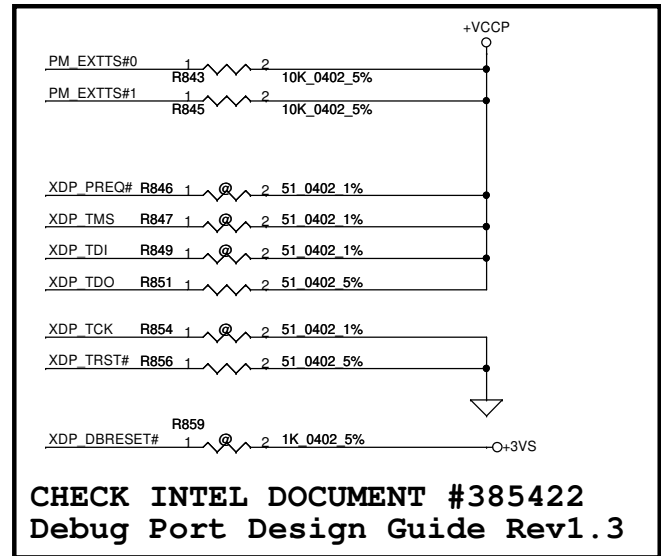
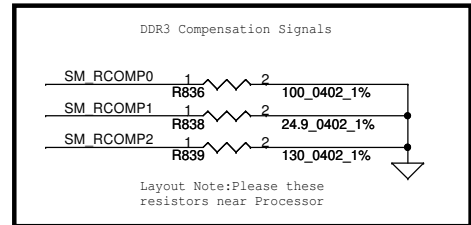
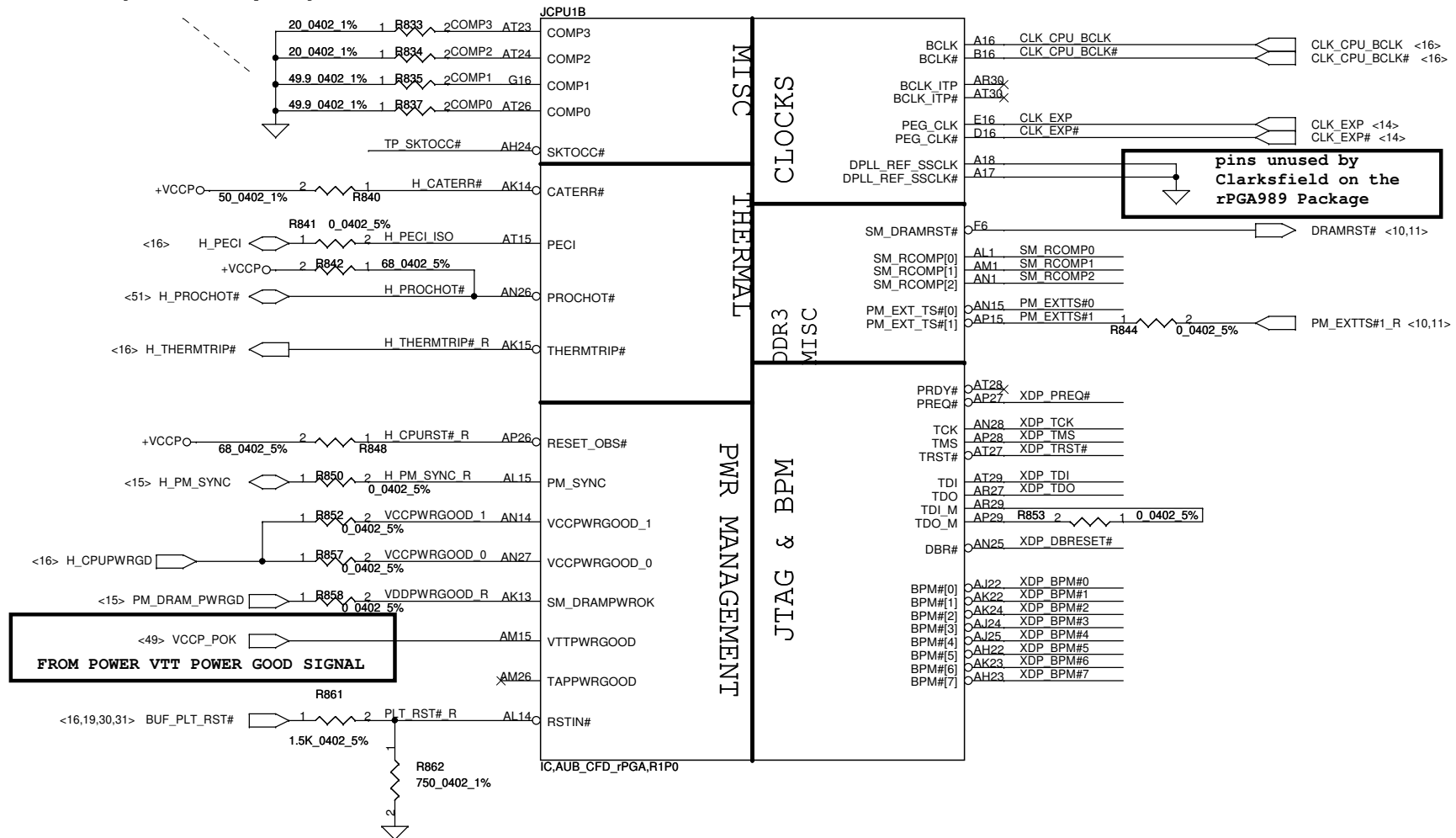
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK (MHz)	NVVDD			FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)		(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10M-GE 64bit 512MB DDR3	13.36	2.93	TBD	TBD	11.89	10.70	0.66	0.99	2.16	3.24	792	0.83	75	0.14	63	0.07	100	0.33
N10M-GS 64bit 512MB DDR3	14.29	3.10	TBD	TBD	11.53	11.53	0.70	1.05	2.28	3.42	817	0.86	75	0.14	63	0.07	100	0.33
N10M-LP 64bit 512MB DDR3	8.28	2.91	TBD	TBD	6.60	5.61	0.62	0.93	2.20	3.3	782	0.82	75	0.14	63	0.07	100	0.33

Power Sequence

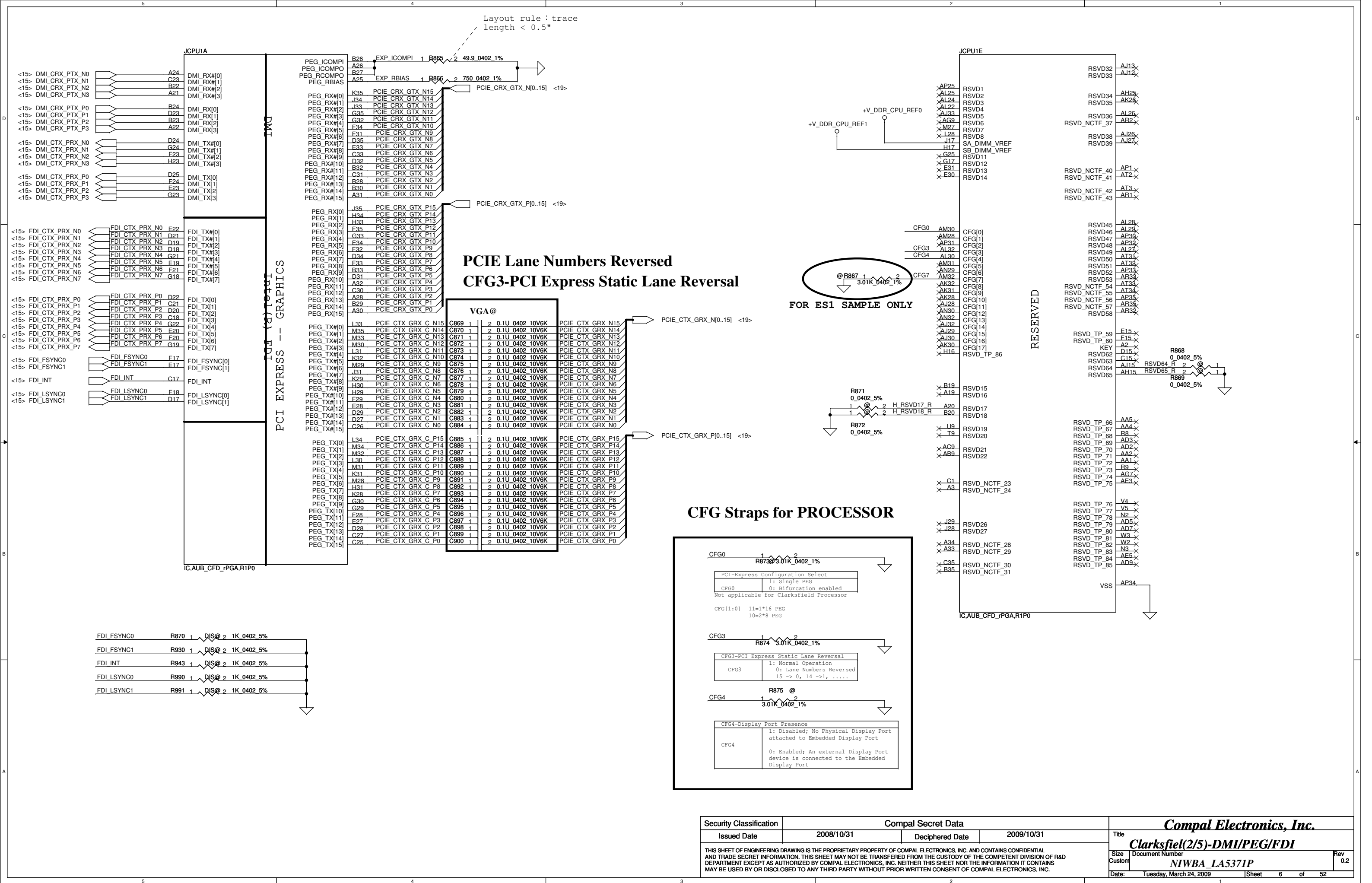
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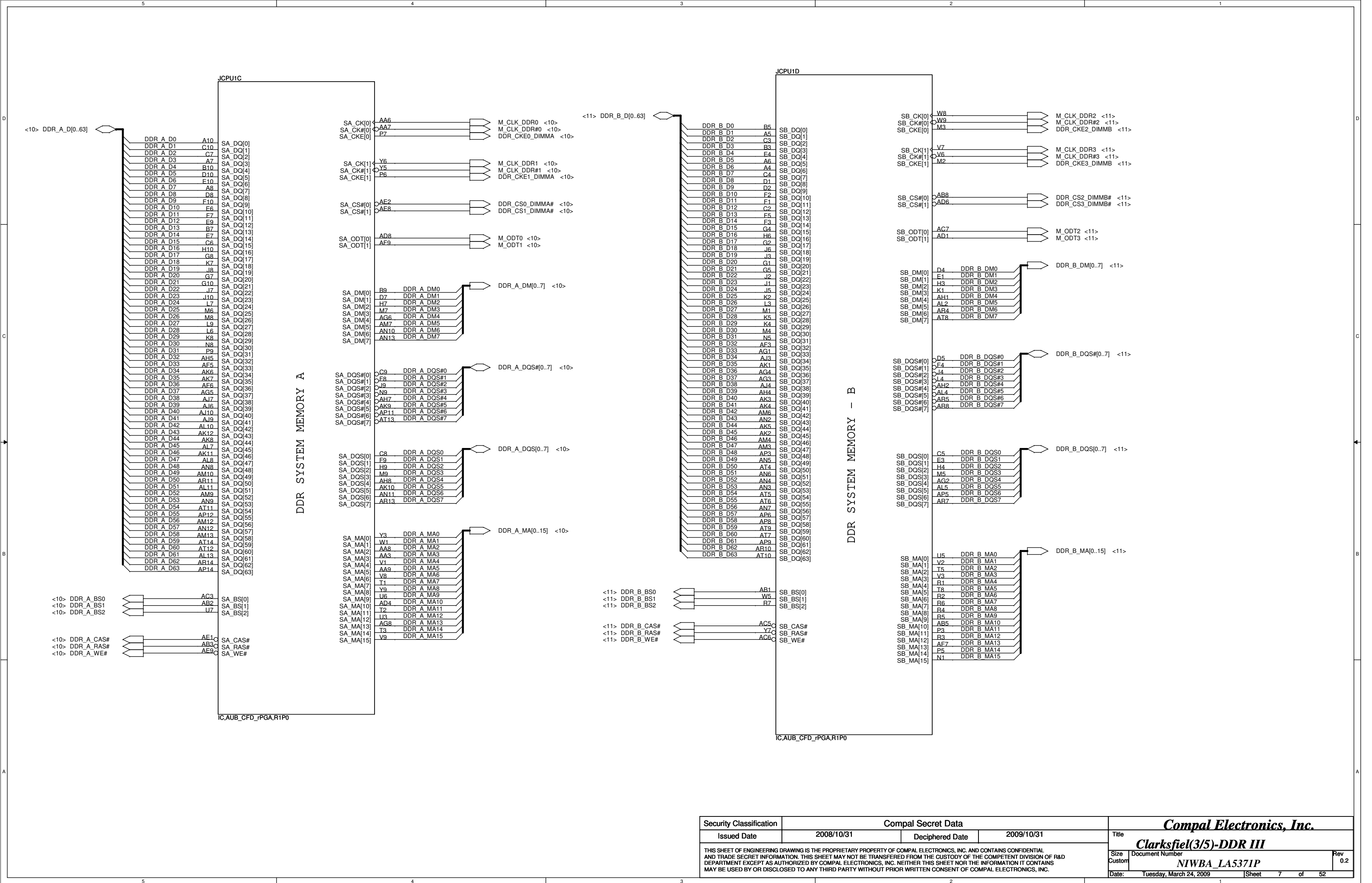


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length < 0.5", spacing 20mil

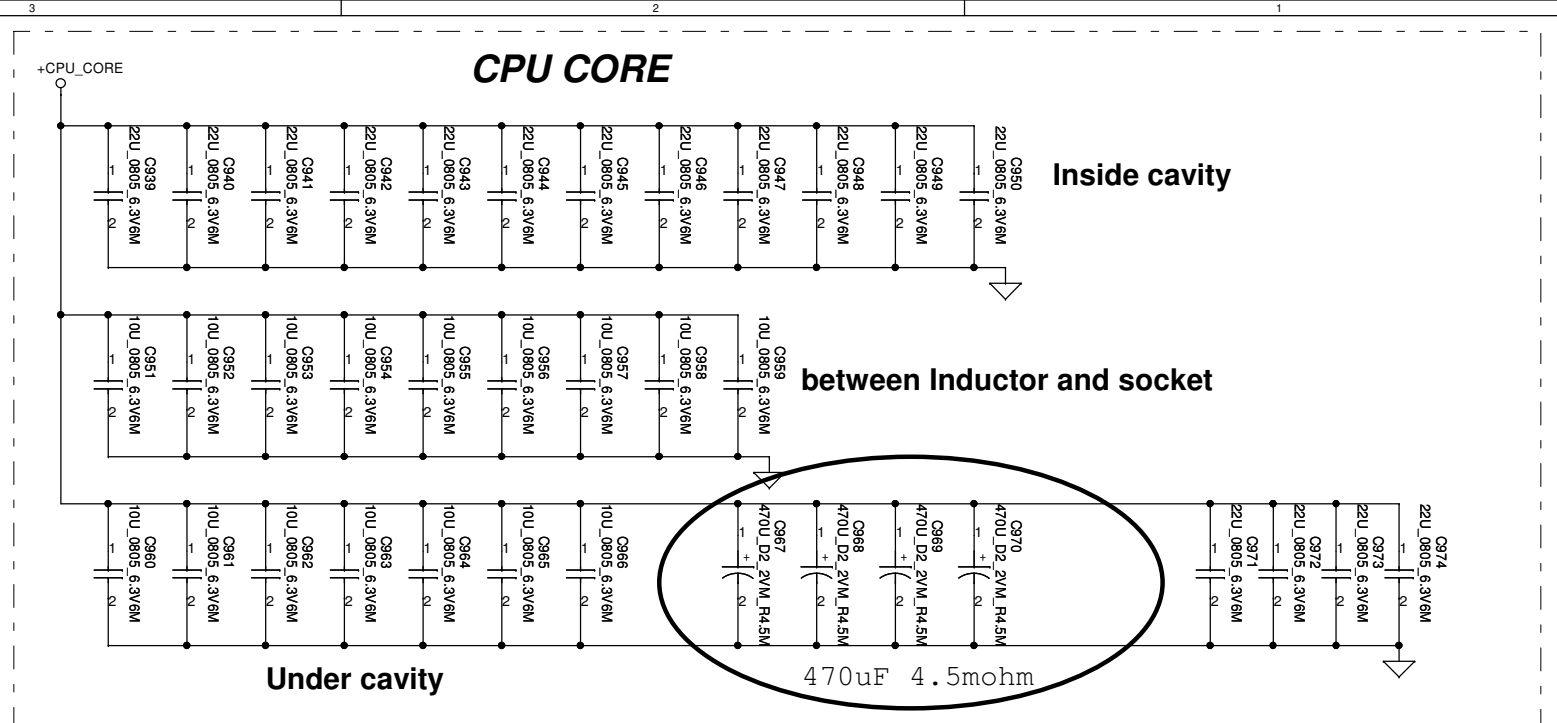
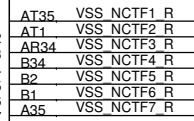
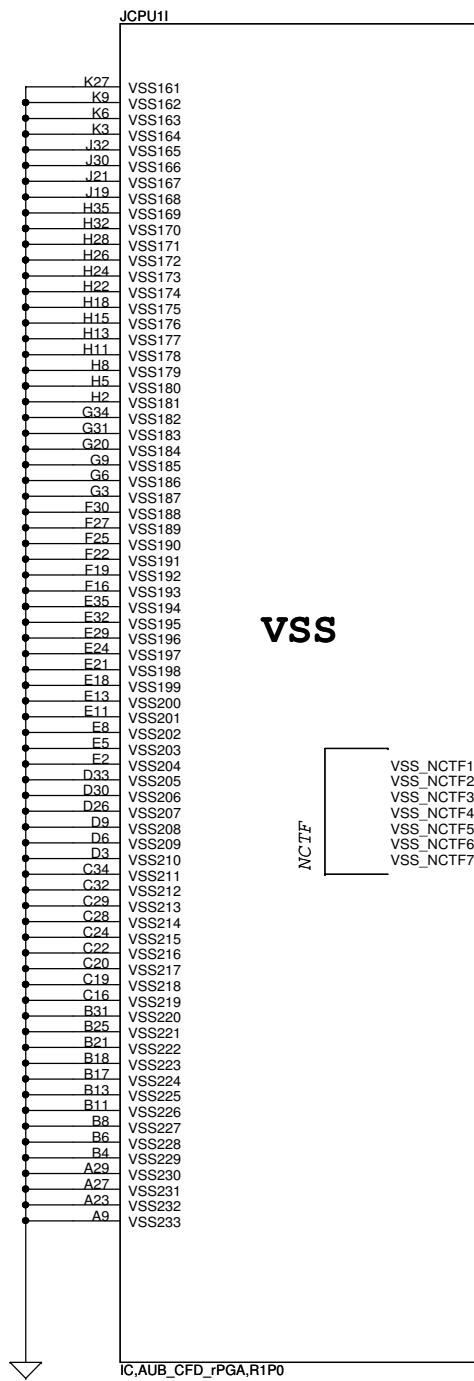
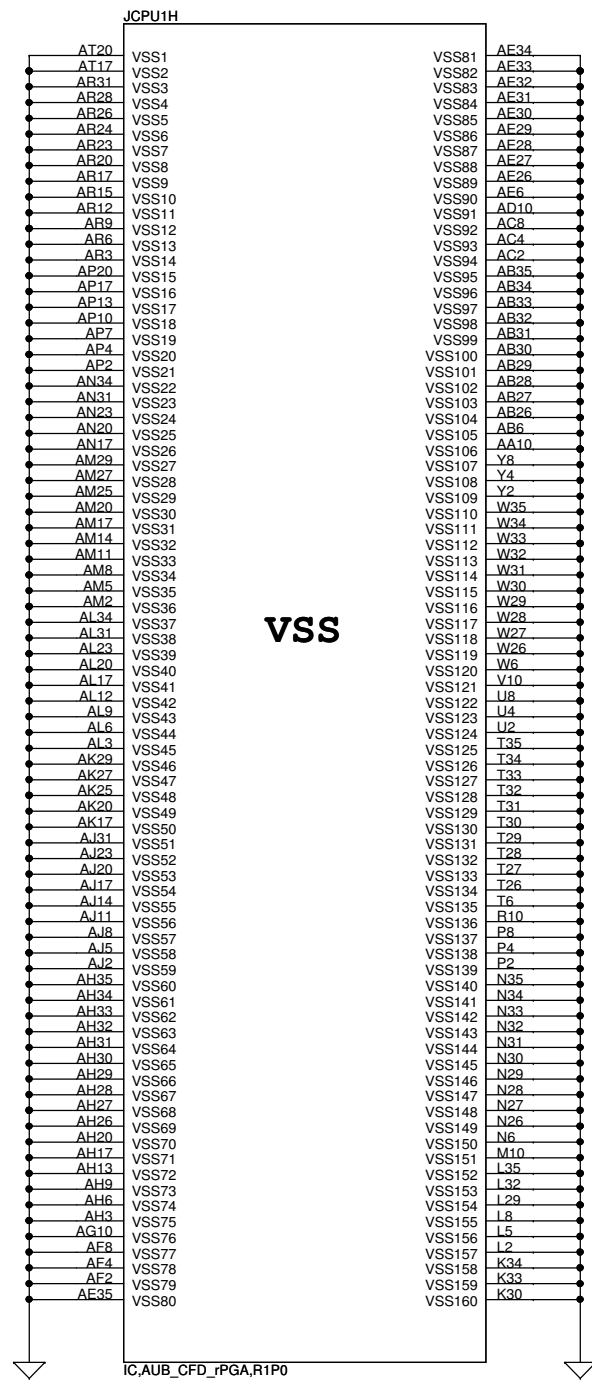


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Size Custom		Document Number NIWBA_LA5371P		Rev 0.2	
Date: Tuesday, March 24, 2009		Sheet 5 of 52			



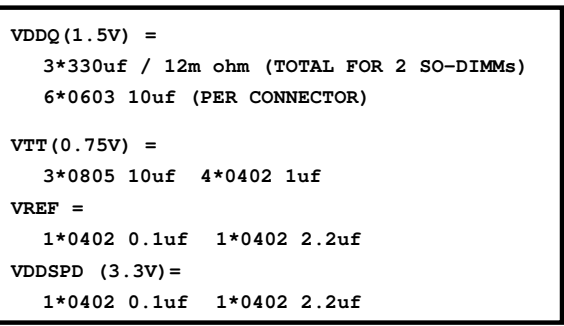


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```
+CPU_CORE = 12*0805 22uf  INSIDE CAVITY
          7*0805 10uf  UNDER CAVITY AND 9*0805 10uf BETWEEN INDUCTOR AND SOCKET ON TOP LAYER
          4*470uf/4m ohm 2*470uf
```

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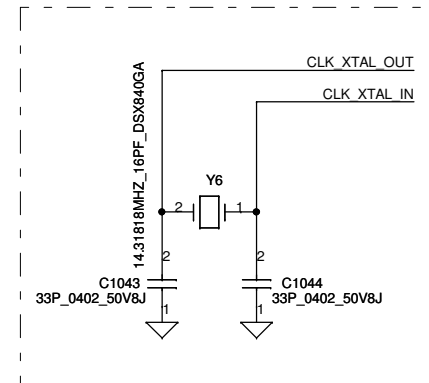
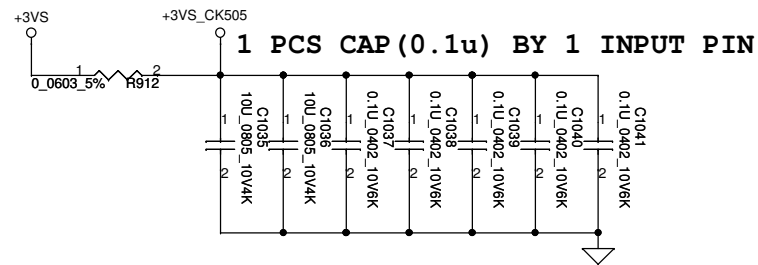
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Issued Date	2008/10/31	Deciphered Date	2009/10/31	Title		
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						Size			
						Date:		Tuesday, March 24, 2009	

1. CLK_DMI
2. CLK_BUF_BCLK
3. CLK_BUF_CKSSCD
4. CLK_BUF_DOT96
5. CLK_14M_PCH

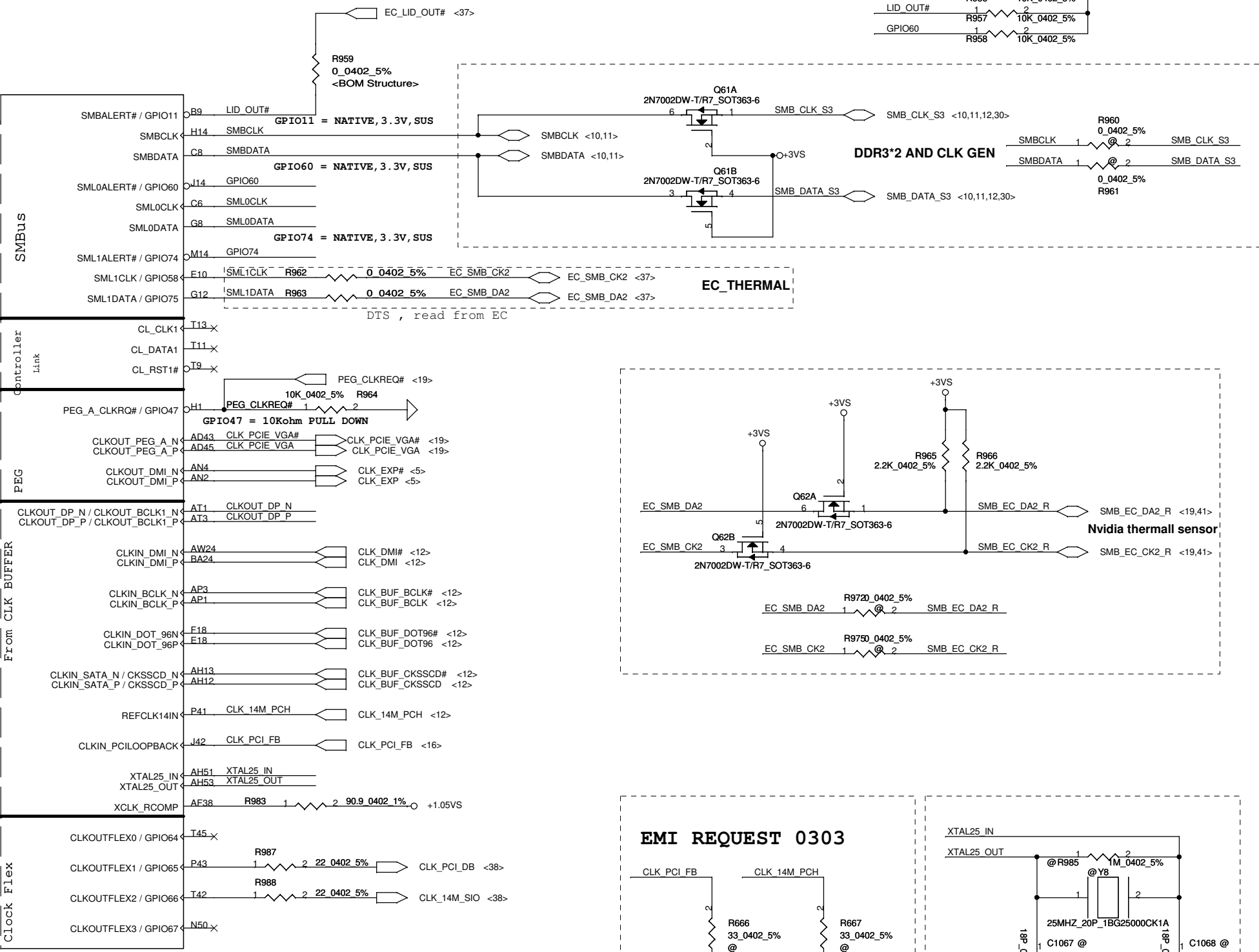
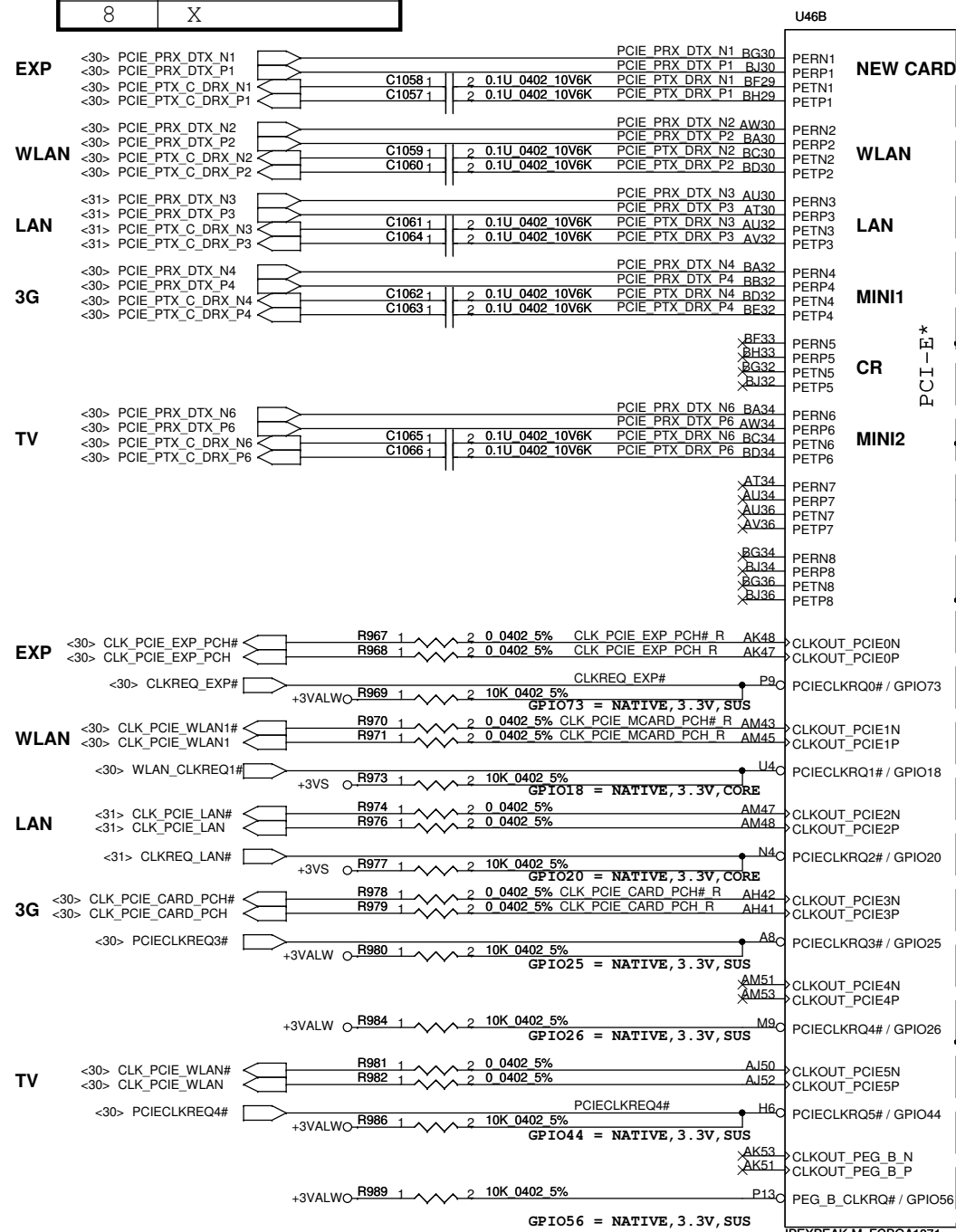
1. 27M_CLK
1. 27M_CLK_SS



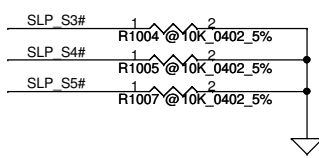
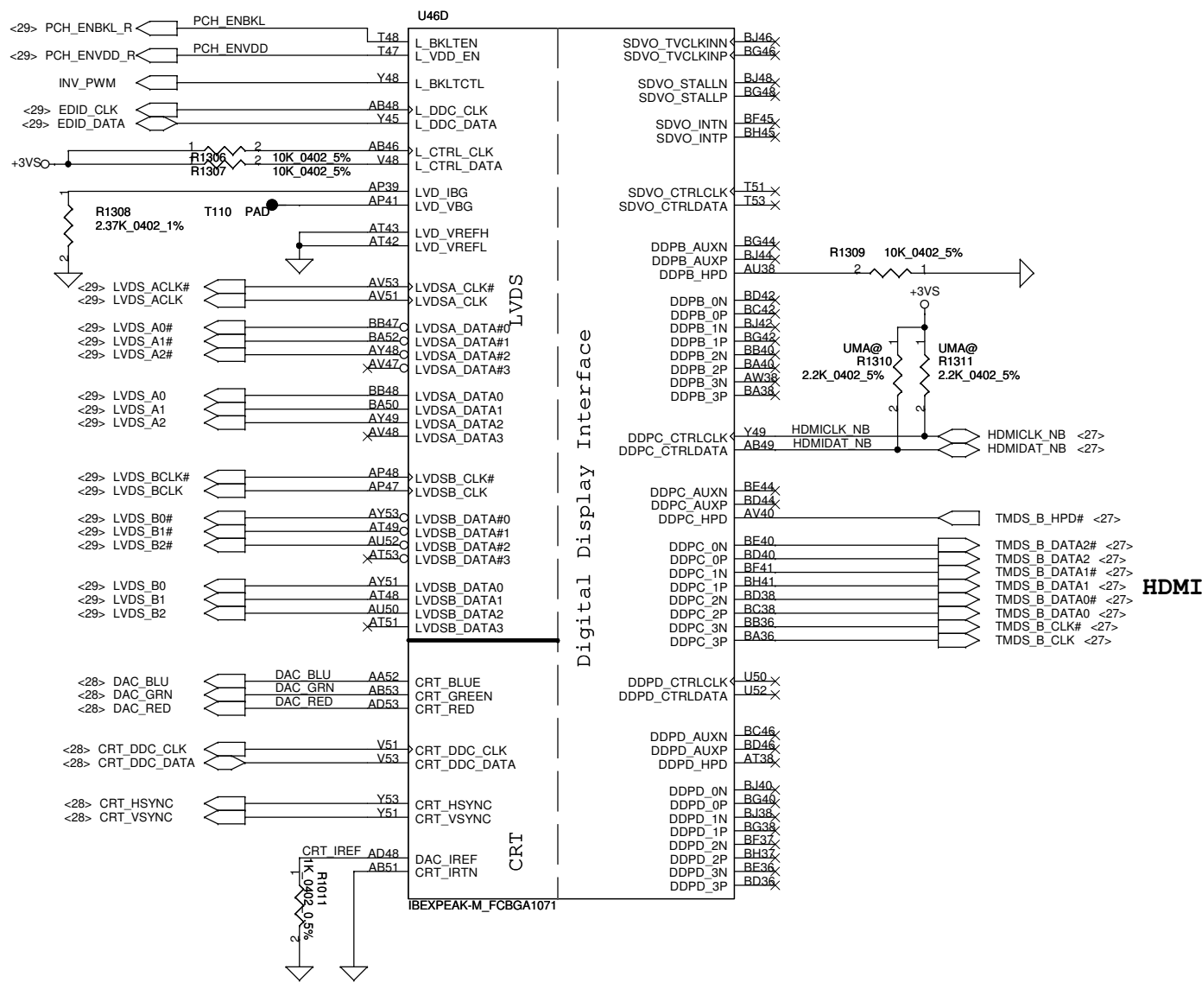
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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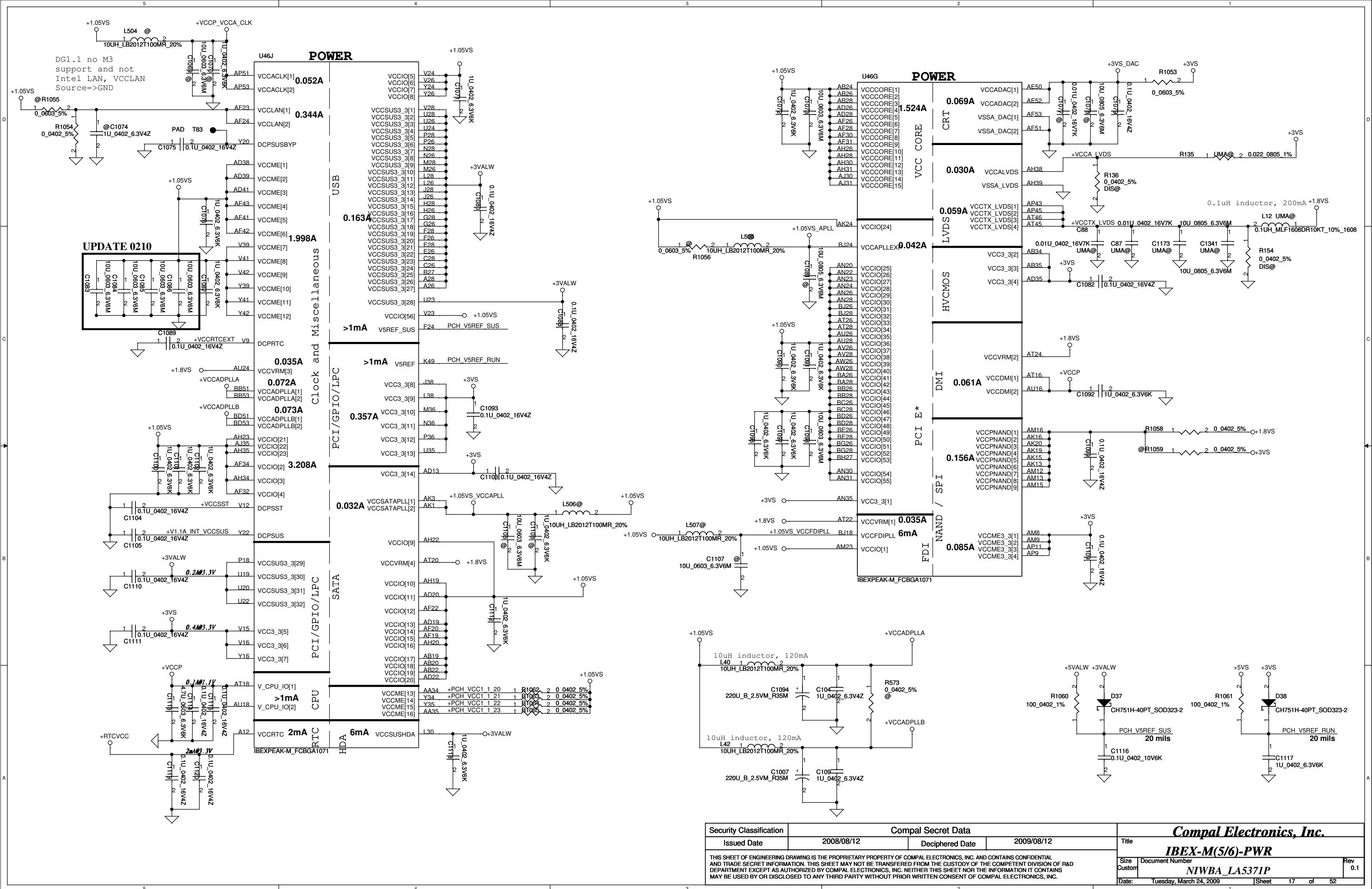
PCIE PORT LIST	
PORT	DEVICE
1	NEW CARD
2	WLAN
3	LAN
4	3G
5	X
6	TV TUNNER
7	X
8	X



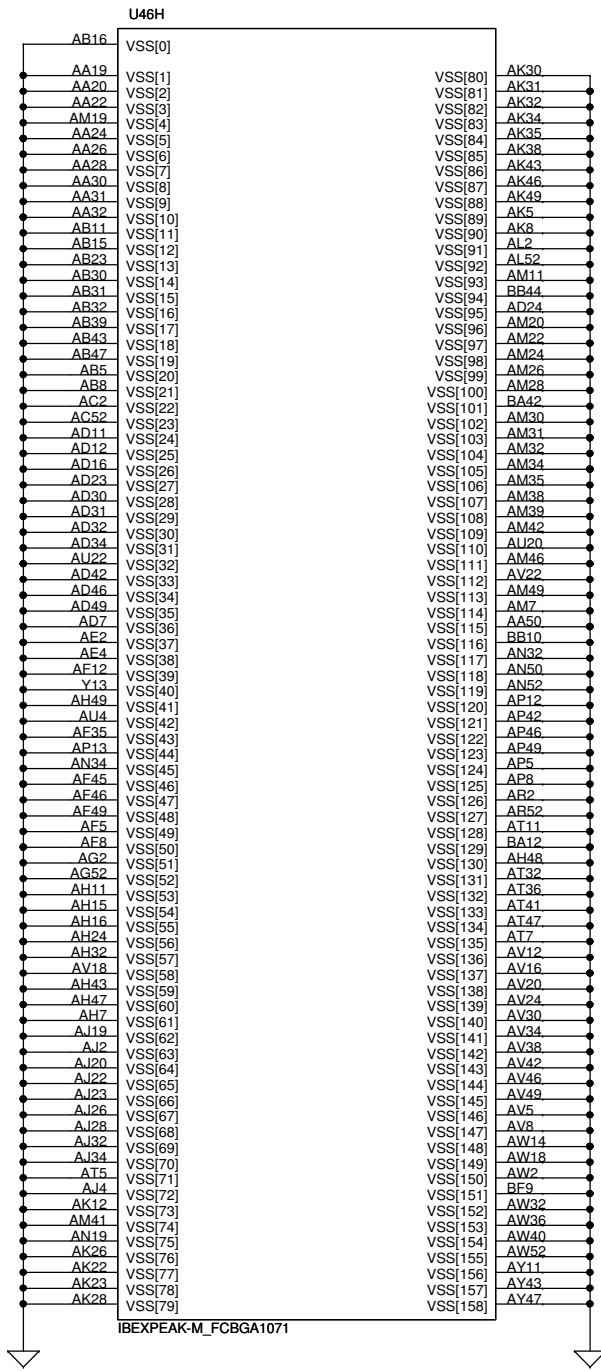
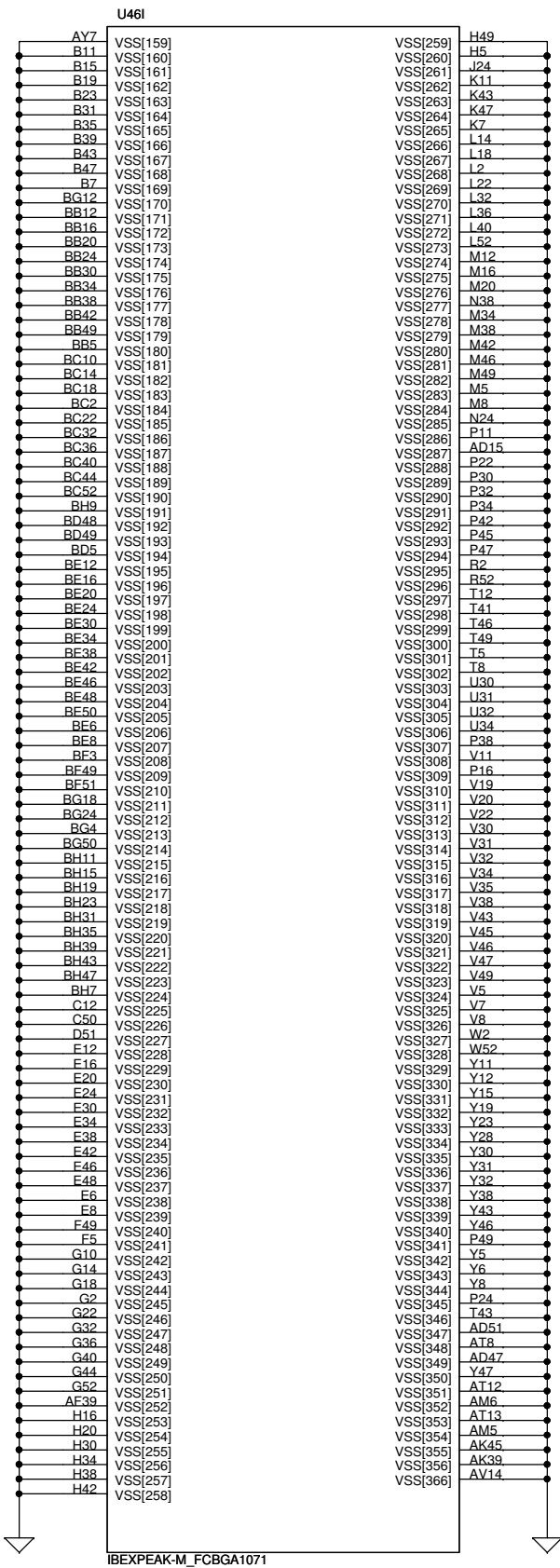
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Date	Tuesday, March 24, 2009	ISheet	14	of	52	



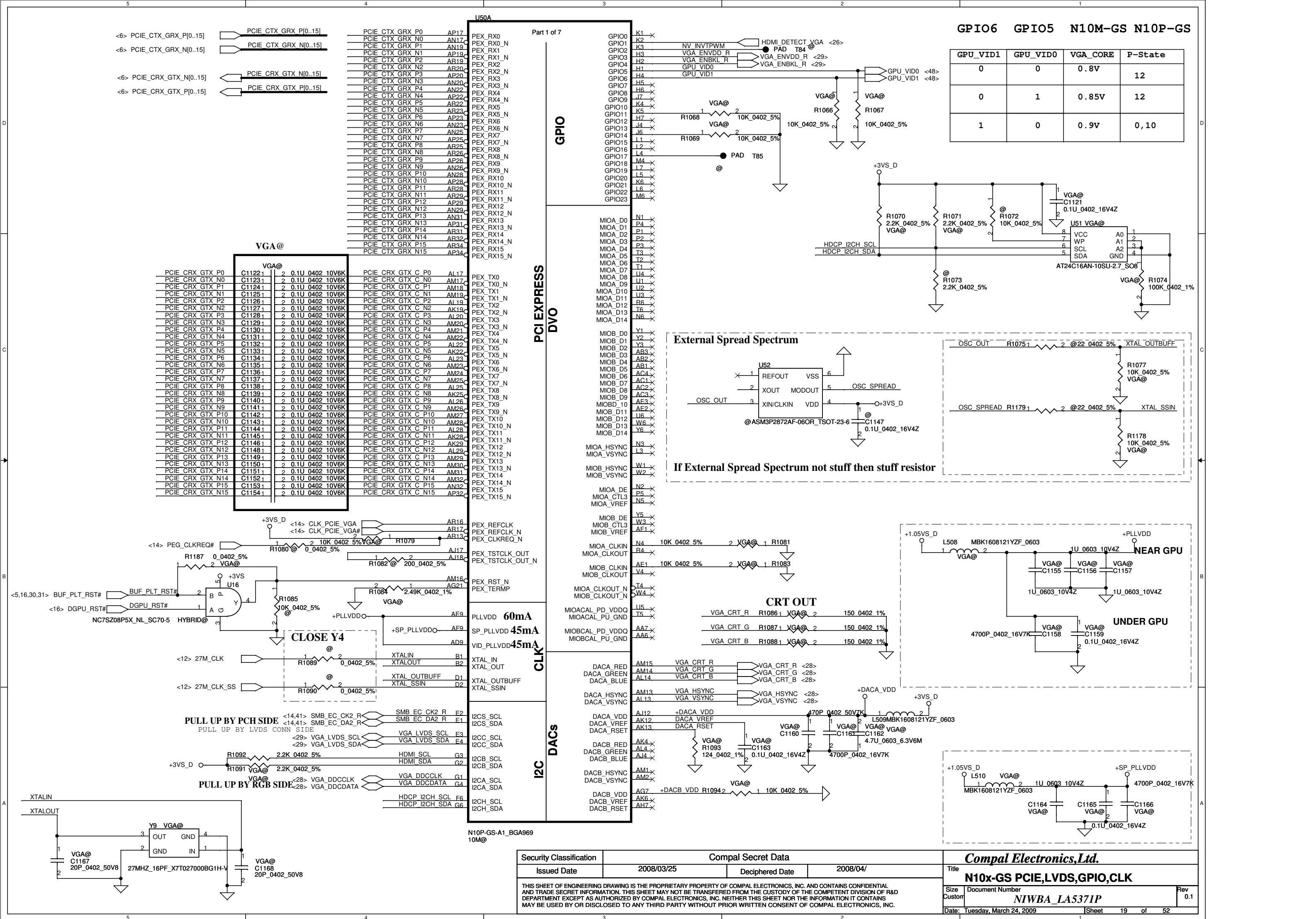
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Date:		Tuesday, March 24, 2009		Sheet	15 of 52

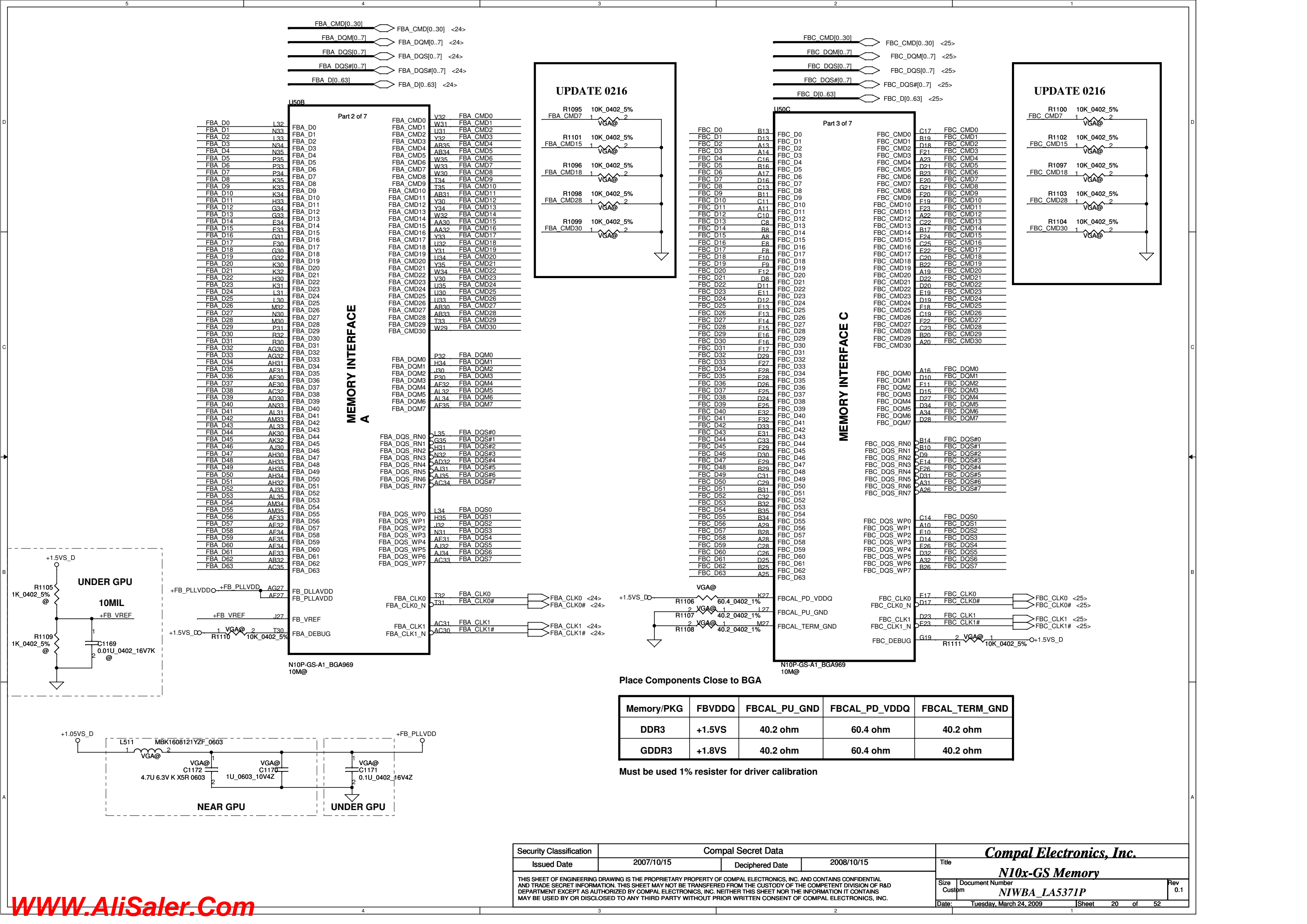


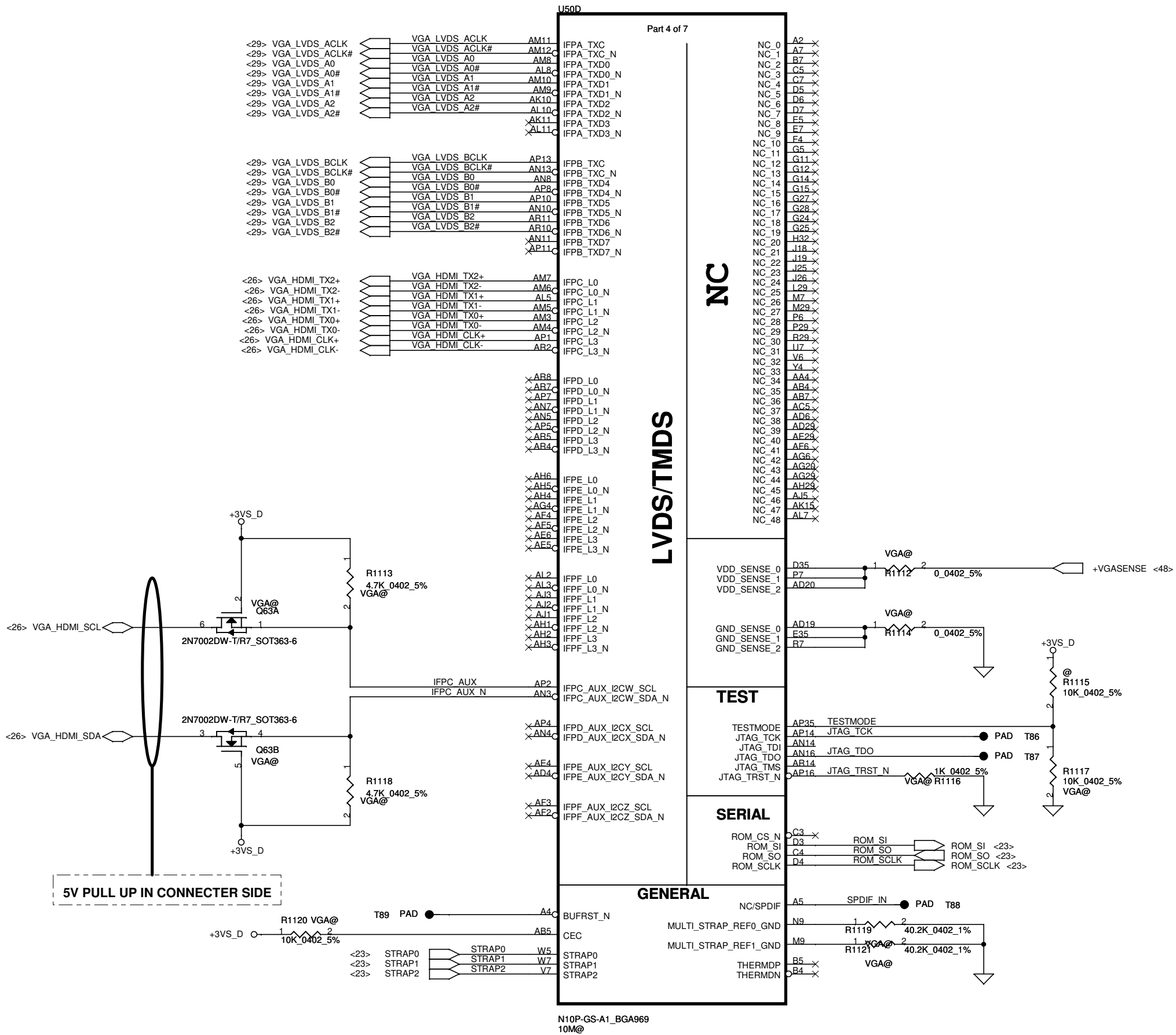
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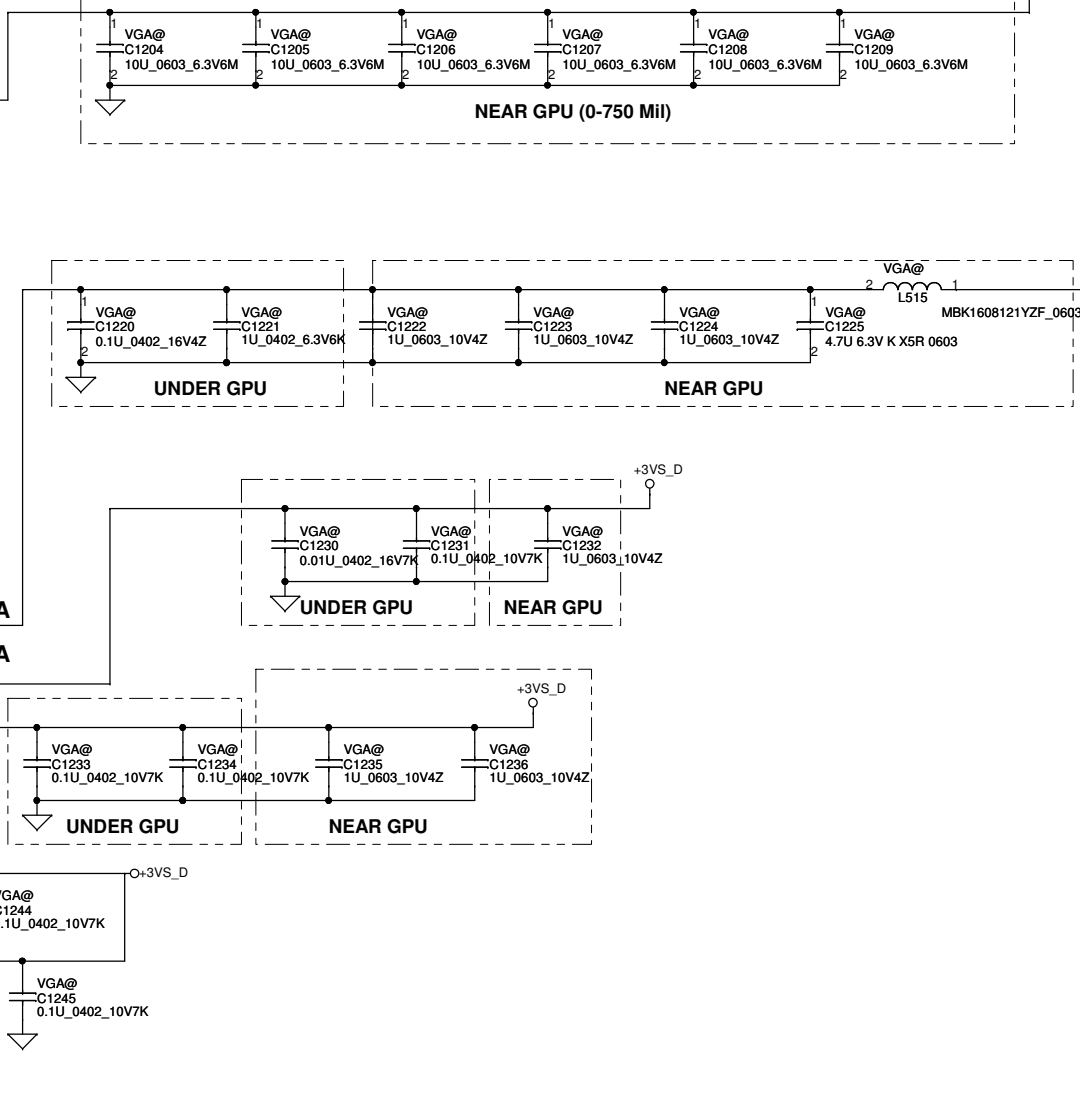
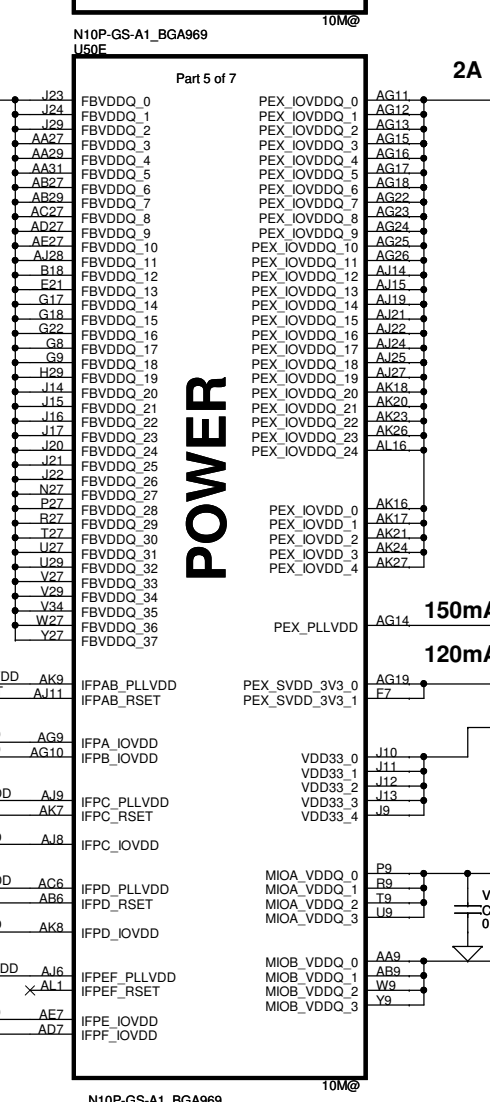
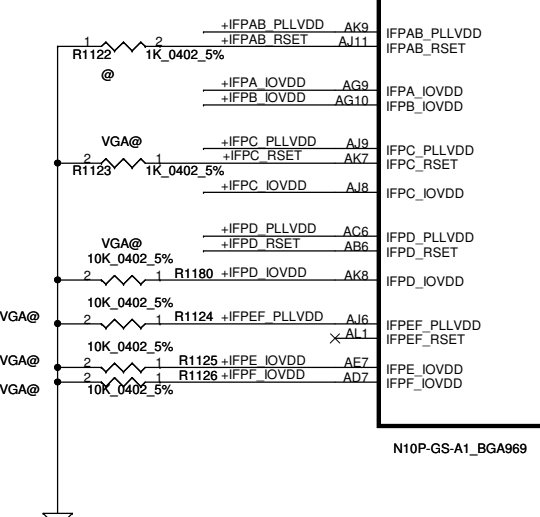
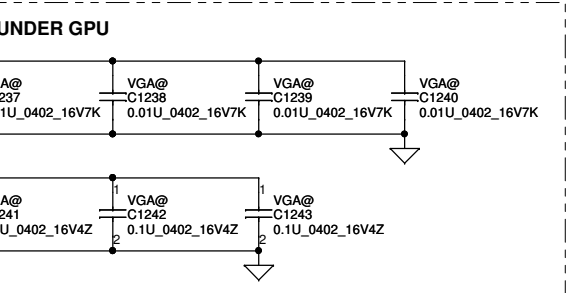
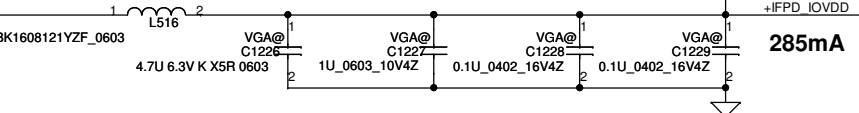
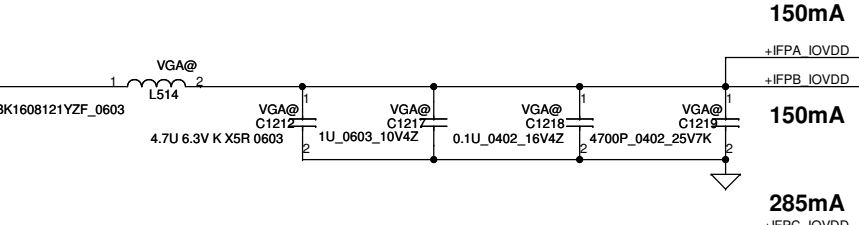
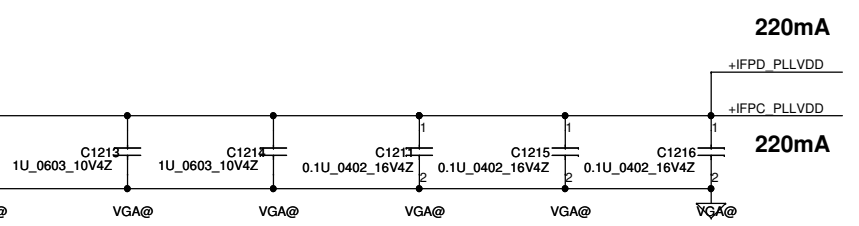
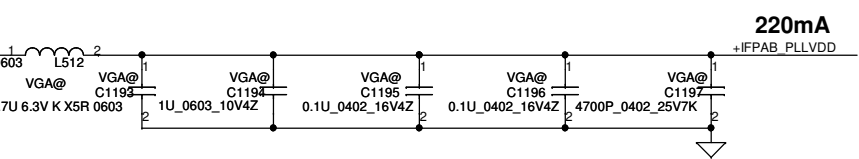
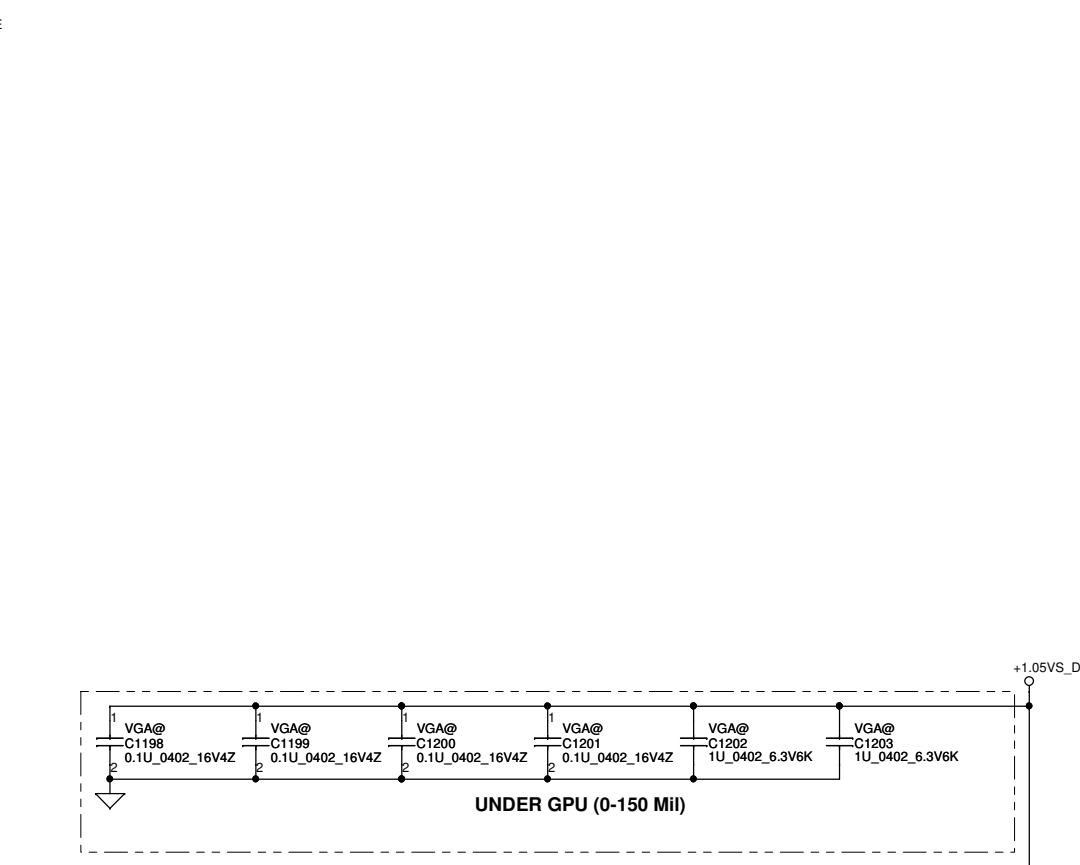
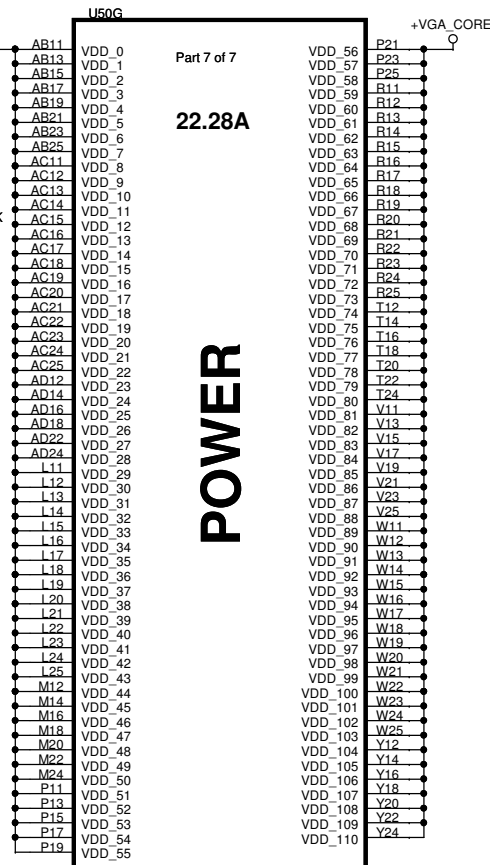
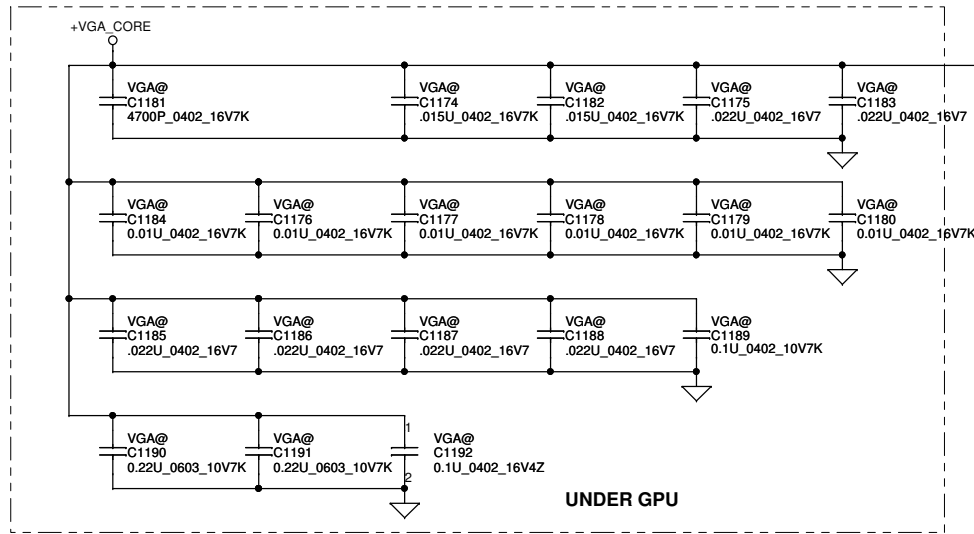


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Issued Date	2008/10/31	Deciphered Date	2009/10/31	Title IBEX-M(6/6)-GND		
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				Date:	Tuesday, March 24, 2009	Sheet 18 of 52

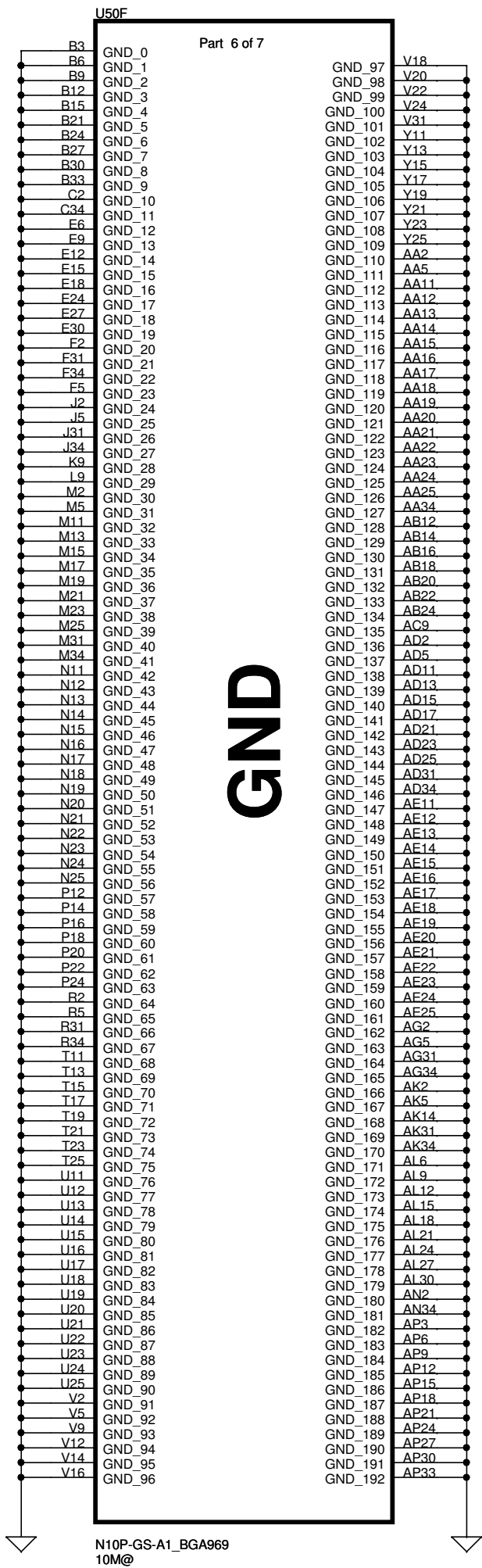




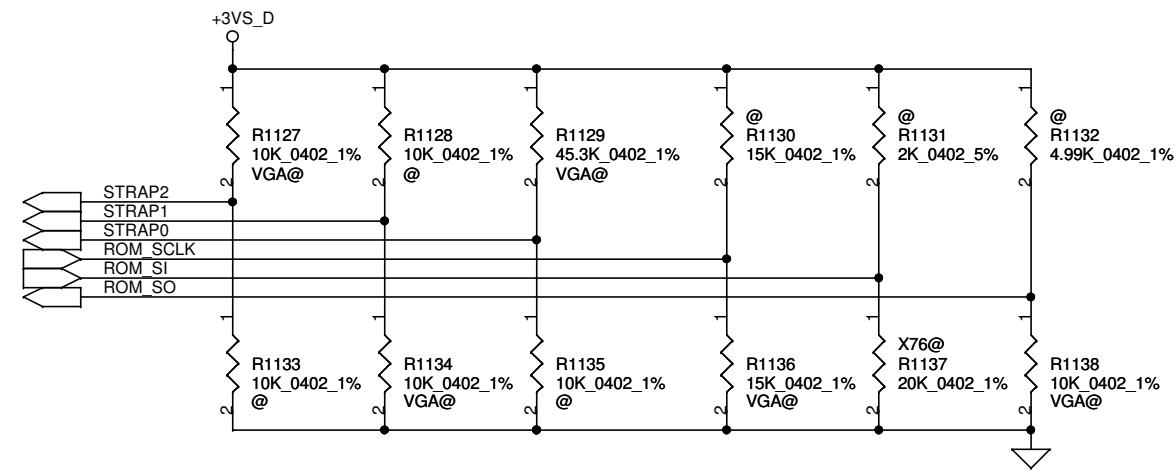
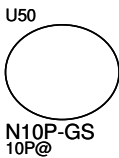
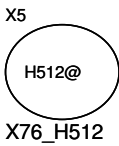
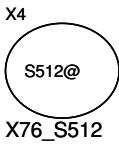
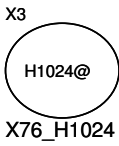
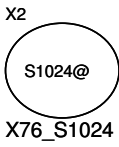




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Issued Date			Deciphered Date			Title		
2007/10/15			2008/10/15			N10x-GS POWER		
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						NIWBA_LA5371P		
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						Sheet 22 of 52		



<21> STRAP2
<21> STRAP1
<21> STRAP0
<21> ROM_SCLK
<21> ROM_SI
<21> ROM_SO



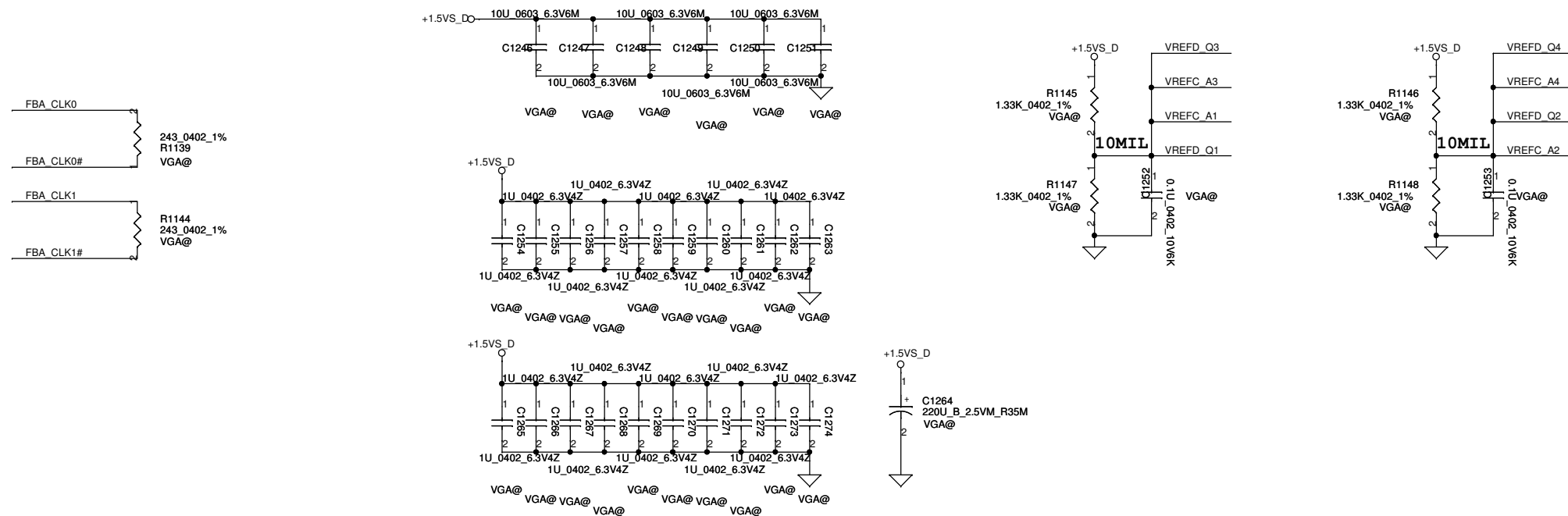
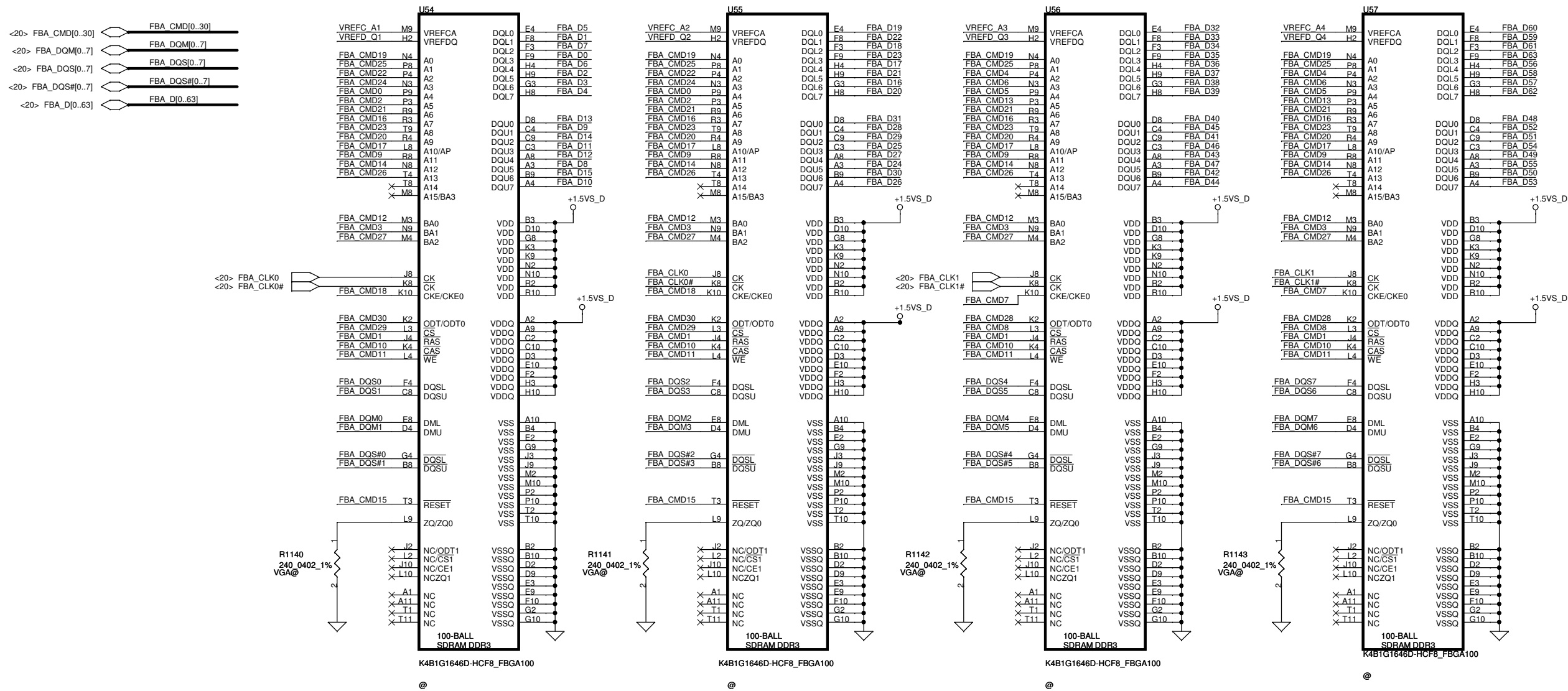
GB1 Family GPU Strap Options

		GPU DEVID	RAM_CFG	GPU DEVID				
GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0	
N10P-GS (0xA34)	Samsung	64Mx16	PD 10K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K

GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0	
N10M-GS (0xA74)	Samsung	64Mx16	PD 10K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K

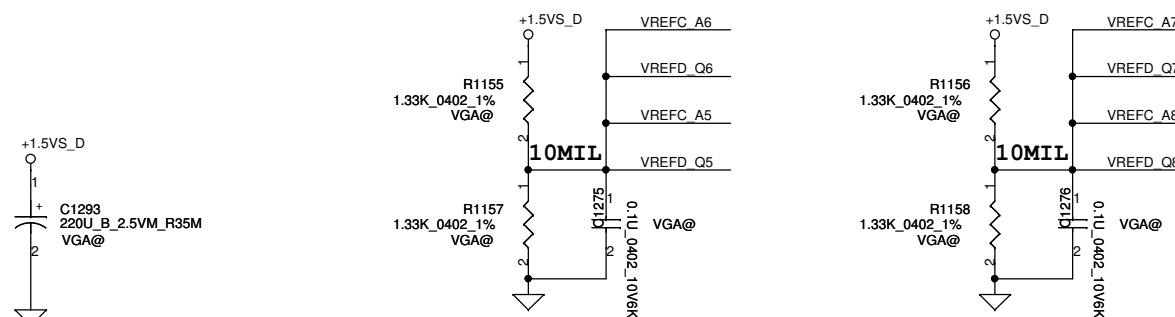
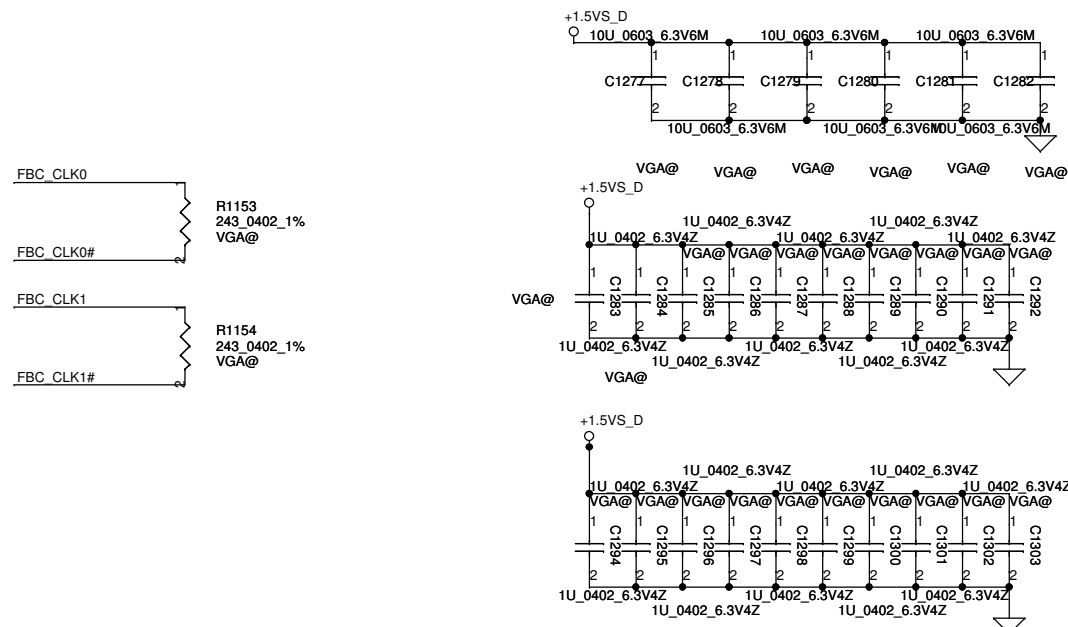
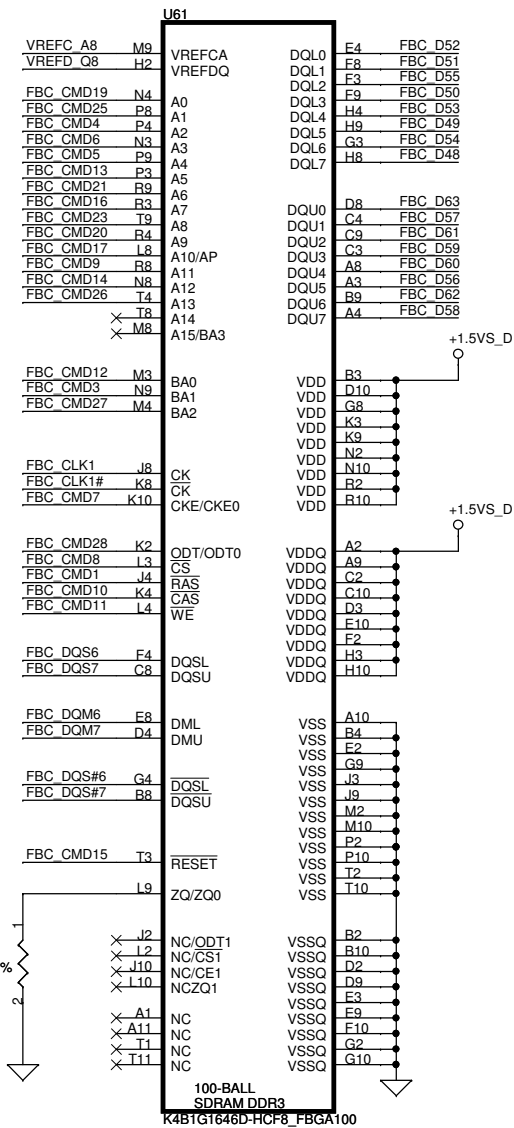
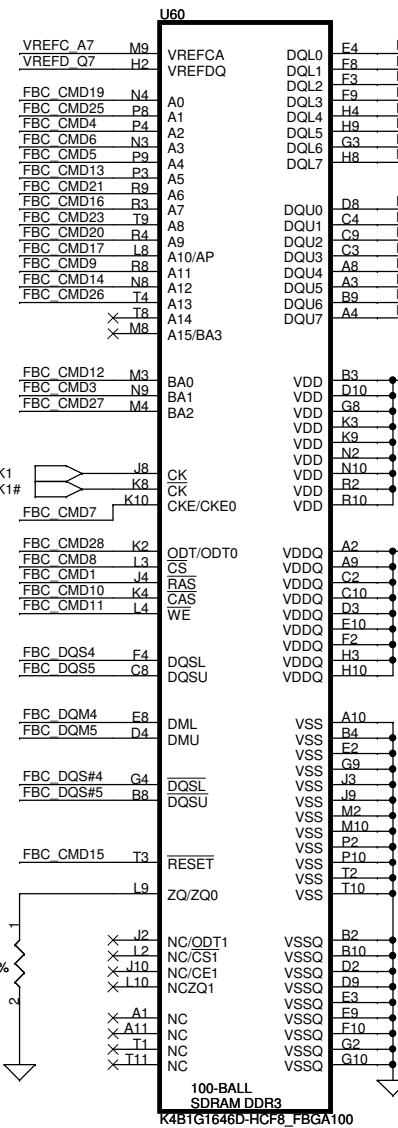
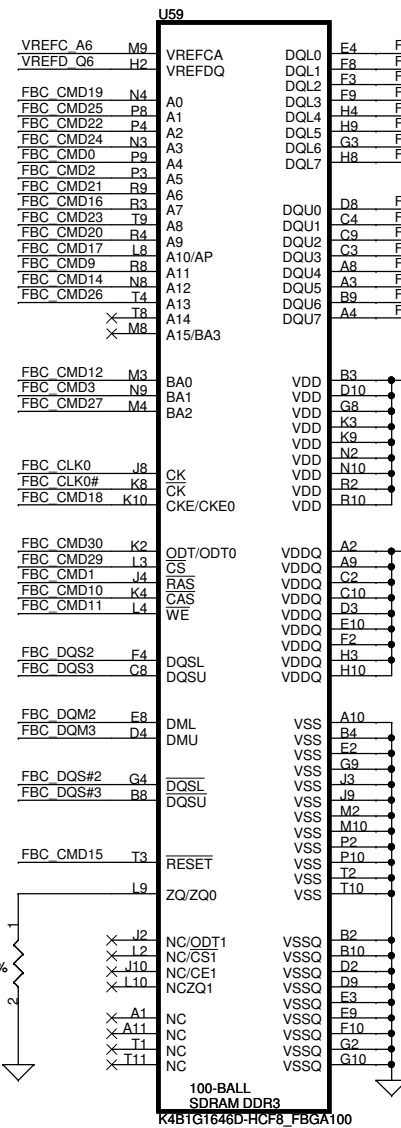
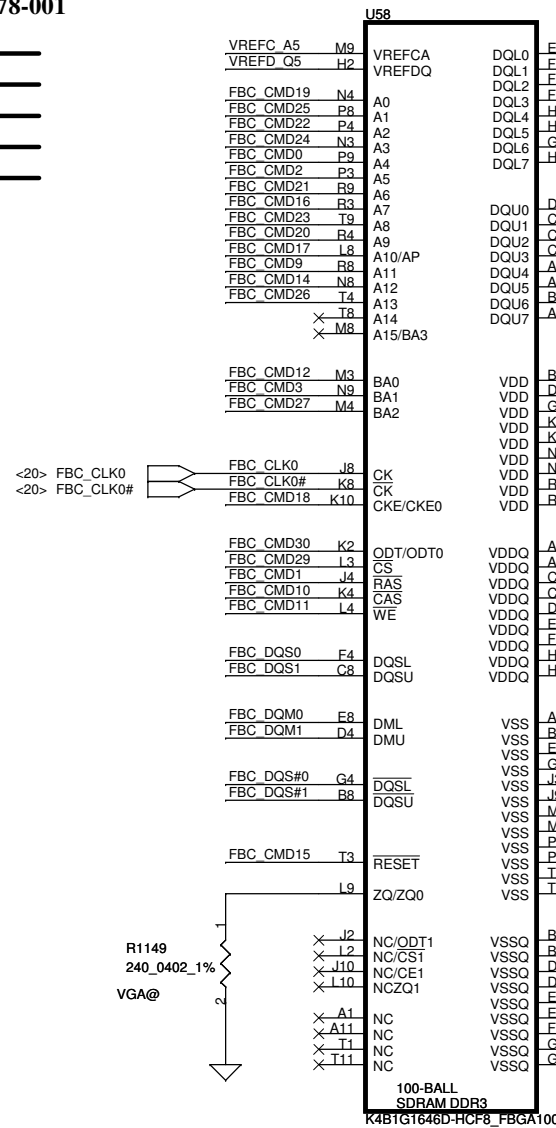
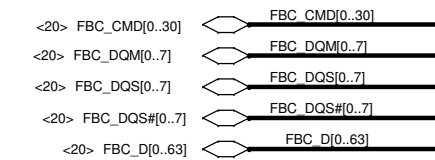
Security Classification	Compal Secret Data			Compal Electronics, Ltd.	
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title N10x-GS GND & STRAP	
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				Date: Tuesday, March 24, 2009	Rev 0.1
		Sheet	23	of	52

N10x 40nm DDR3 MAPPING
NVIDIA COCUMENT FOR DA-3978-001



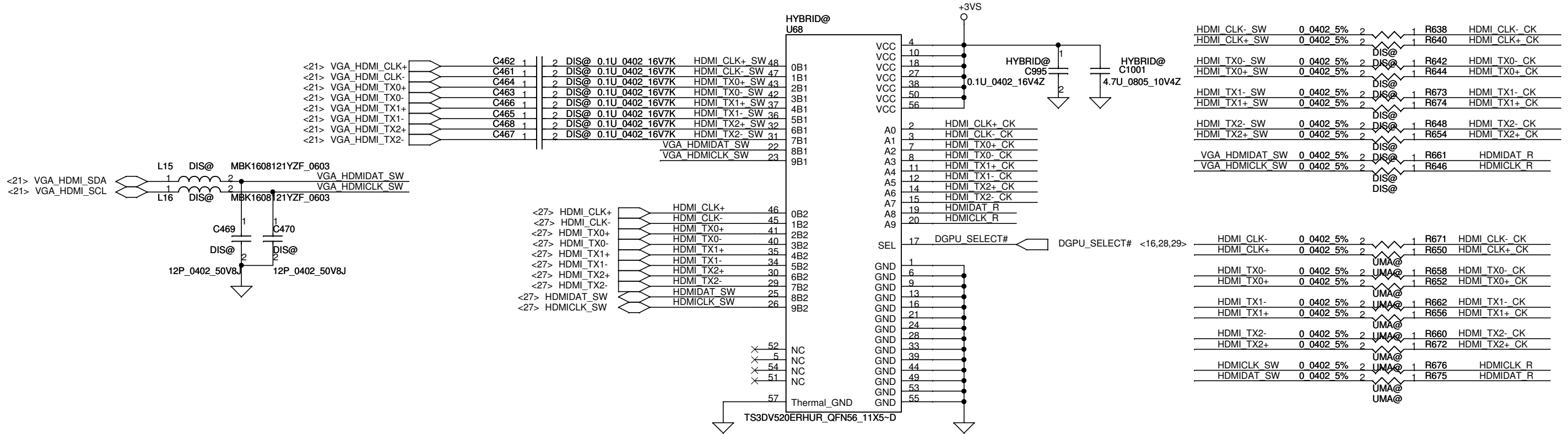
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title		
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				Size C	Document Number	Rev 0.1
				NIWBA_LA5371P		
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N10x 40nm DDR3 MAPPING
NVIDIA COCUMENT FOR DA-3978-001

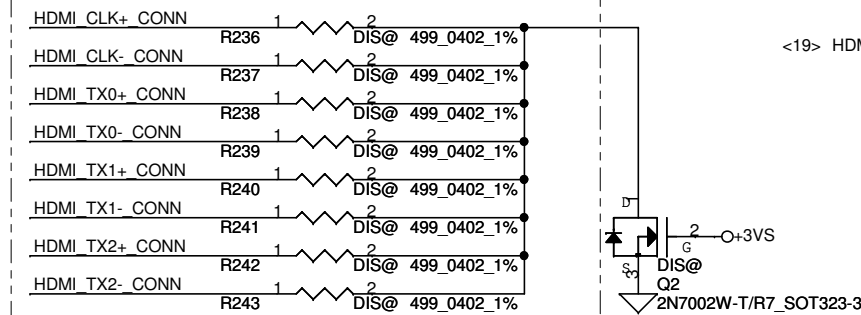


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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title VRAM DDRA		
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				Custom	NIWBA_LA5371P	0.1
Date:				Tuesday, March 24, 2009	Sheet	25 of 52

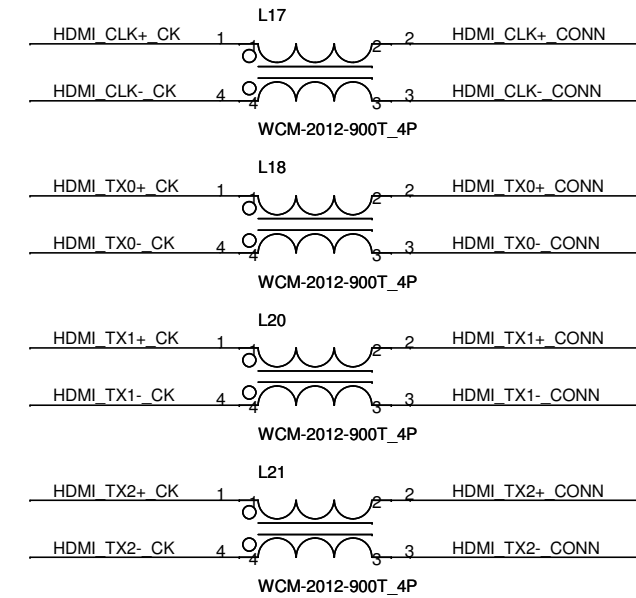
HDMI switch1



TMDS pull down (500ohm) resistors G9x only

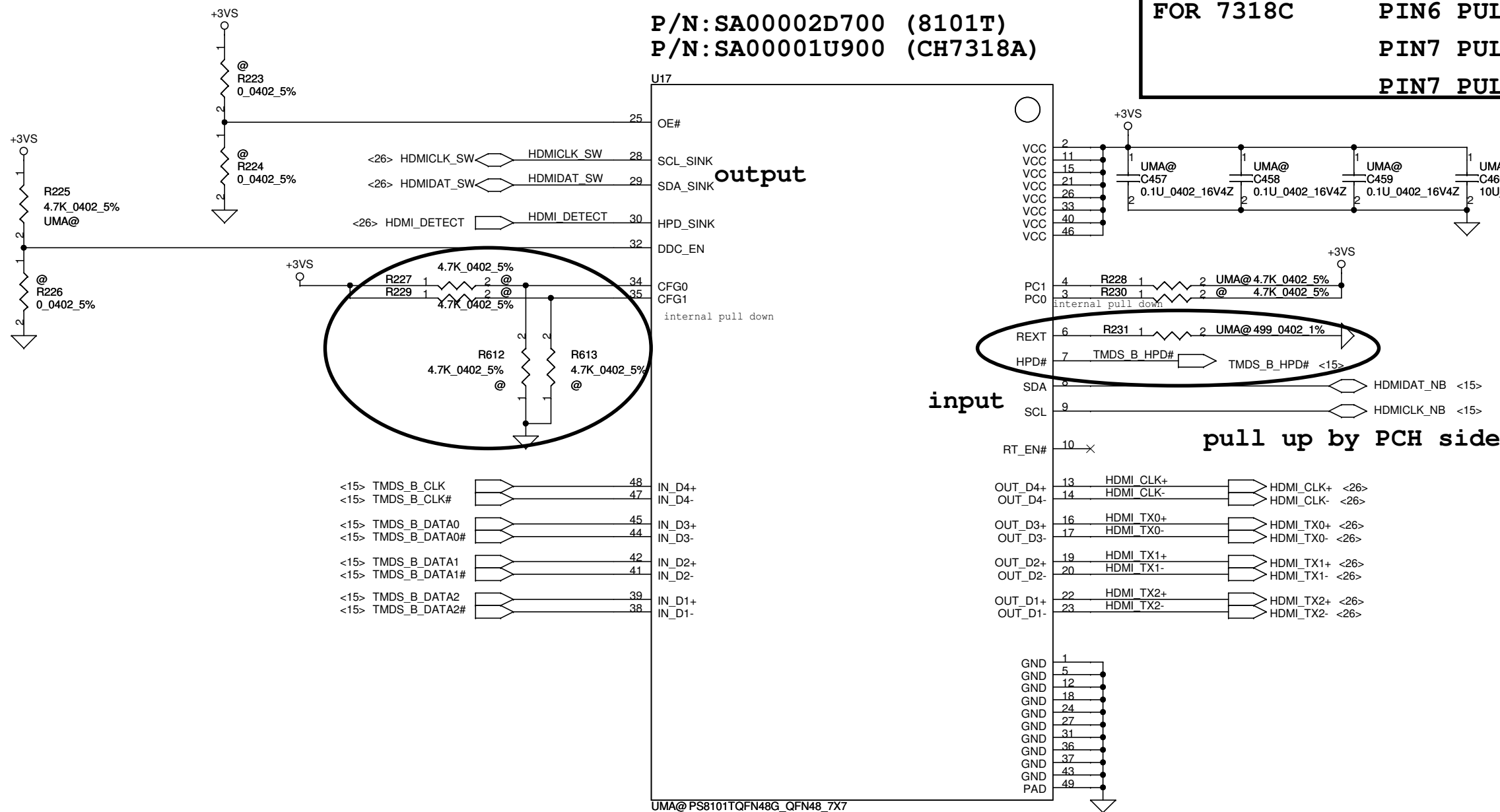


NEAR CONNECT

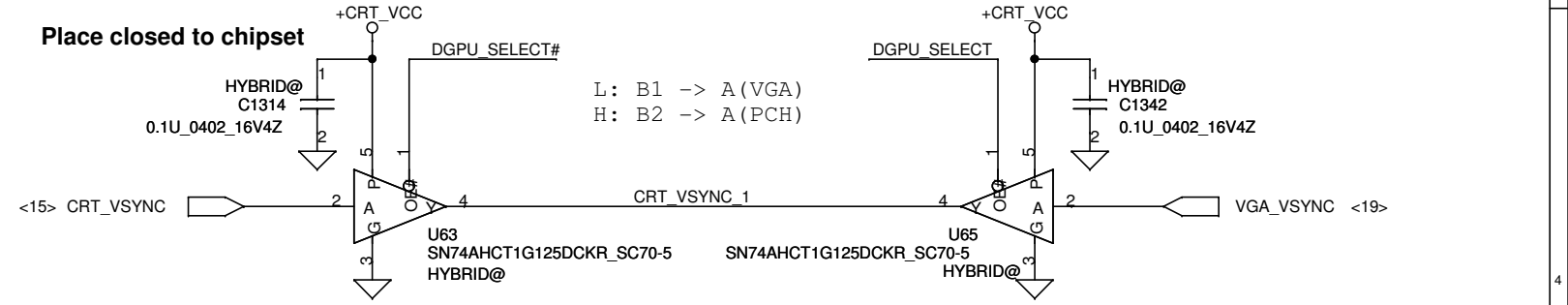
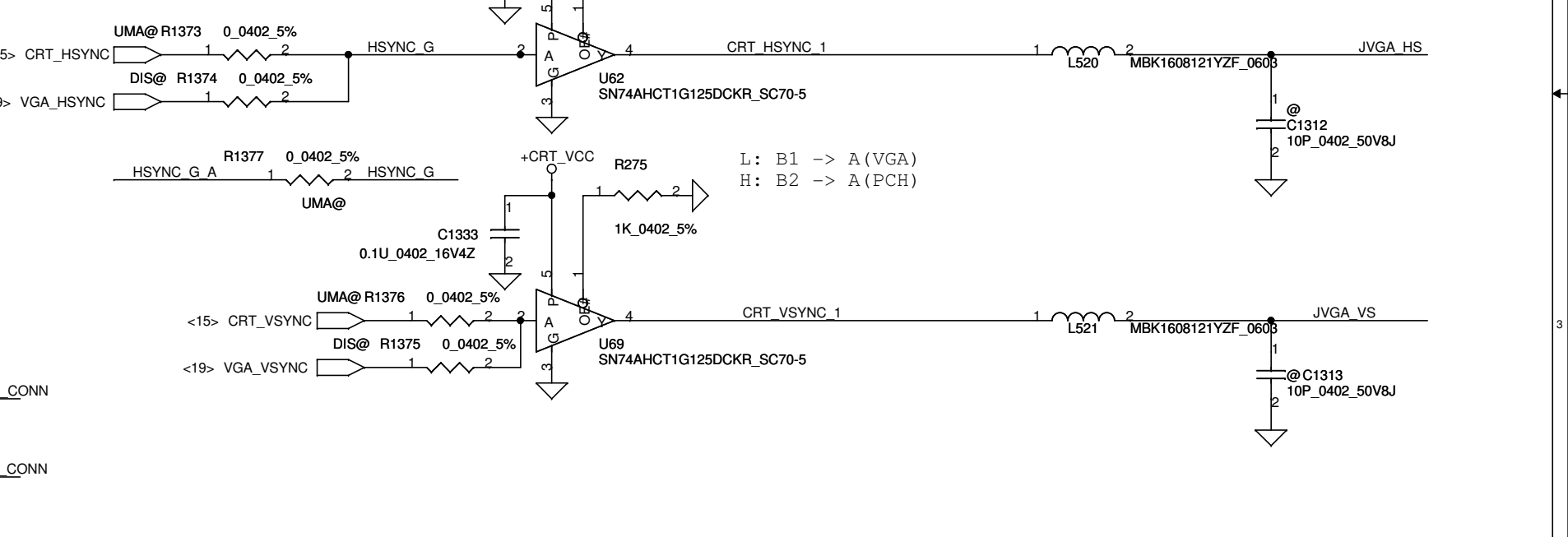
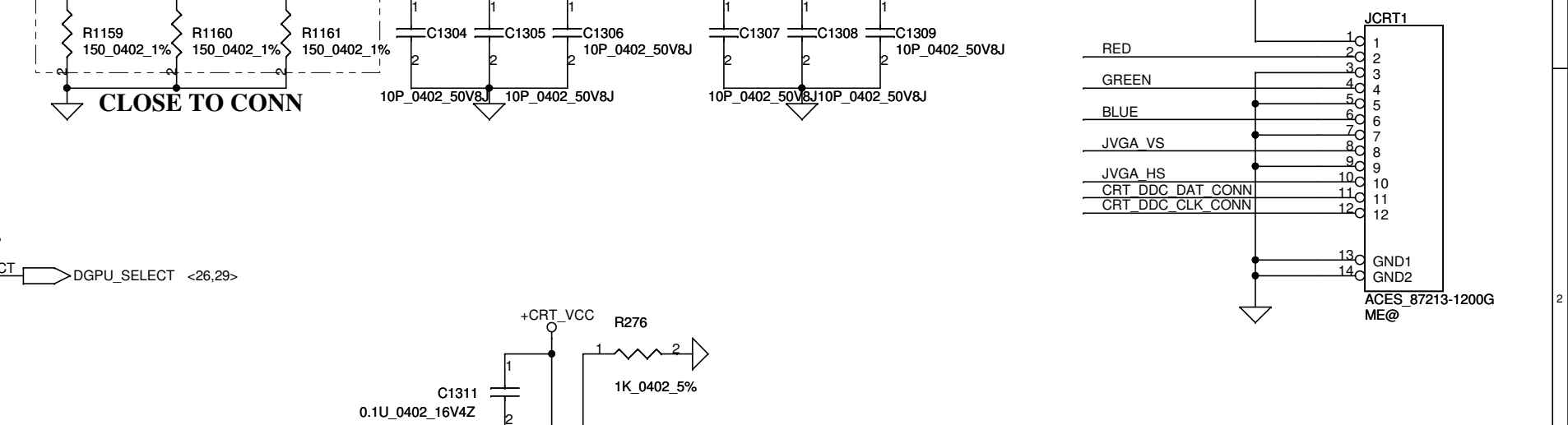
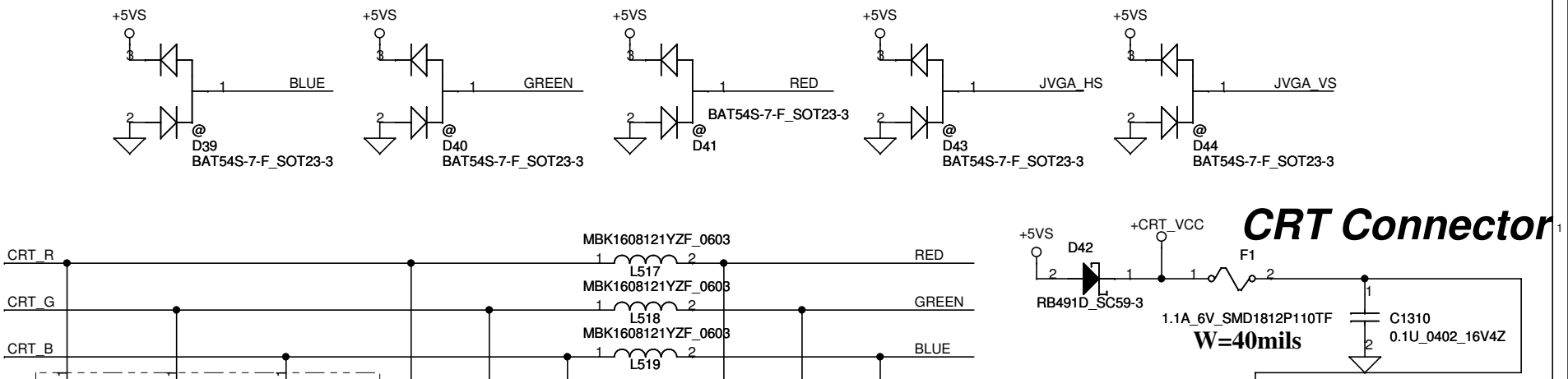
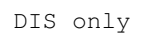
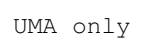


HDMI CLK+ CK	R251	1	@	2	0	0402	5%	HDMI CLK+ CONN
HDMI CLK- CK	R252	1	@	2	0	0402	5%	HDMI CLK- CONN
HDMI TX0+ CK	R253	1	@	2	0	0402	5%	HDMI TX0+ CONN
HDMI TX0- CK	R254	1	@	2	0	0402	5%	HDMI TX0- CONN
HDMI TX1+ CK	R255	1	@	2	0	0402	5%	HDMI TX1+ CONN
HDMI TX1- CK	R256	1	@	2	0	0402	5%	HDMI TX1- CONN
HDMI TX2+ CK	R257	1	@	2	0	0402	5%	HDMI TX2+ CONN
HDMI TX2- CK	R258	1	@	2	0	0402	5%	HDMI TX2- CONN

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								Level Shiftter_PS8101T			
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								KIWB1/B2_LA4601P			
								Date: Tuesday, March 24, 2009		Sheet 26 of 52	

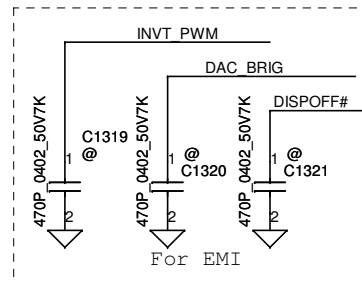
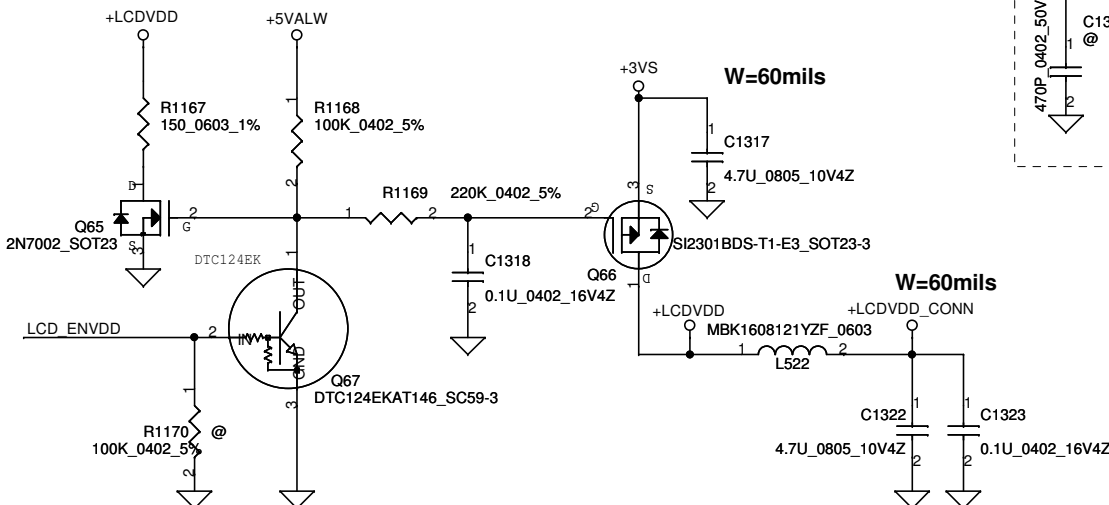


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				Size Custom	Rev 0.1
				Document Number	KIWB1/B2_LA4601P
				Date: Tuesday, March 24, 2009	Sheet 27 of 52

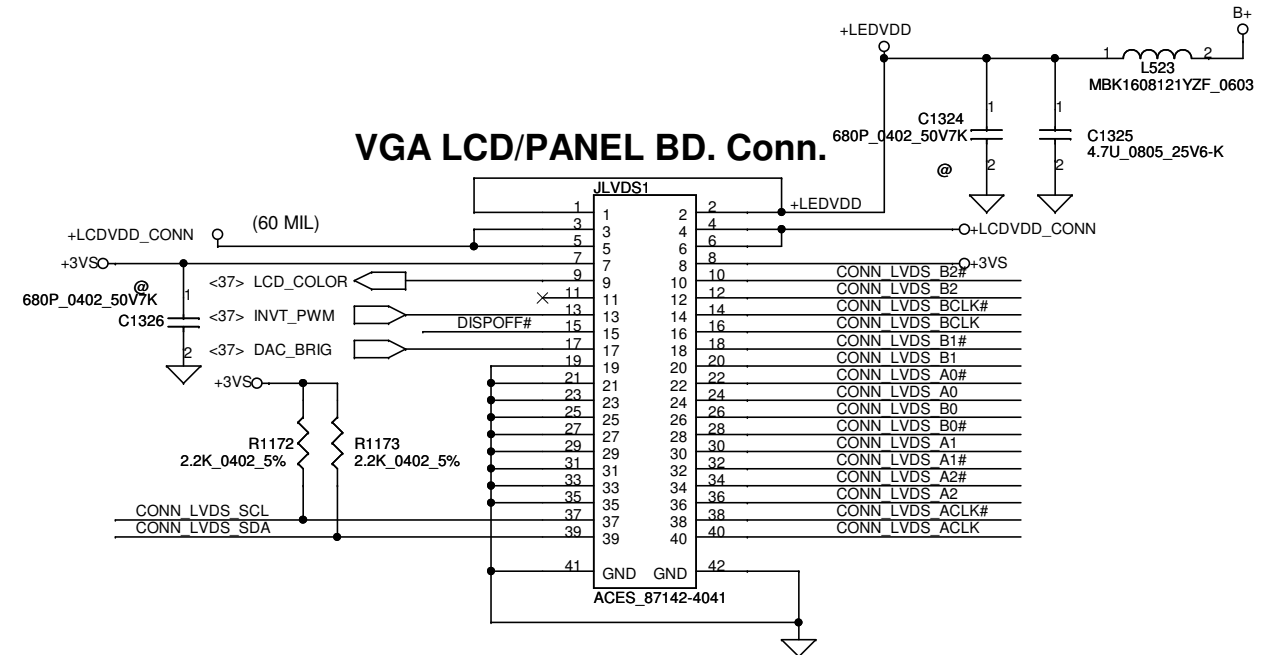


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						Size	Document Number		NIWBA_LA5371P		Rev 0.1
						Custom					
		C		D		Date: Tuesday, March 24, 2009		Sheet 28 of 52			
								E			

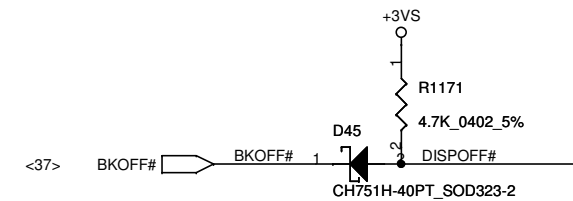
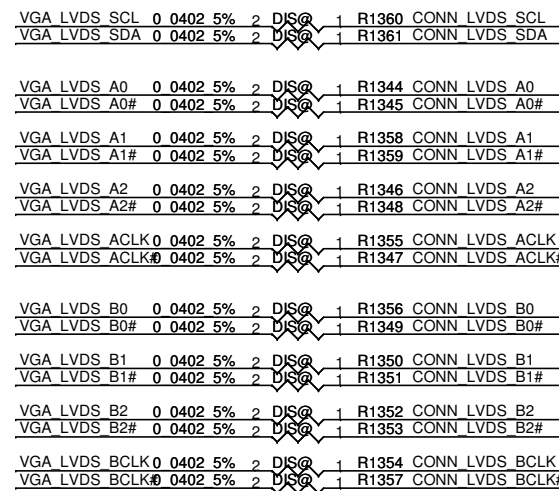
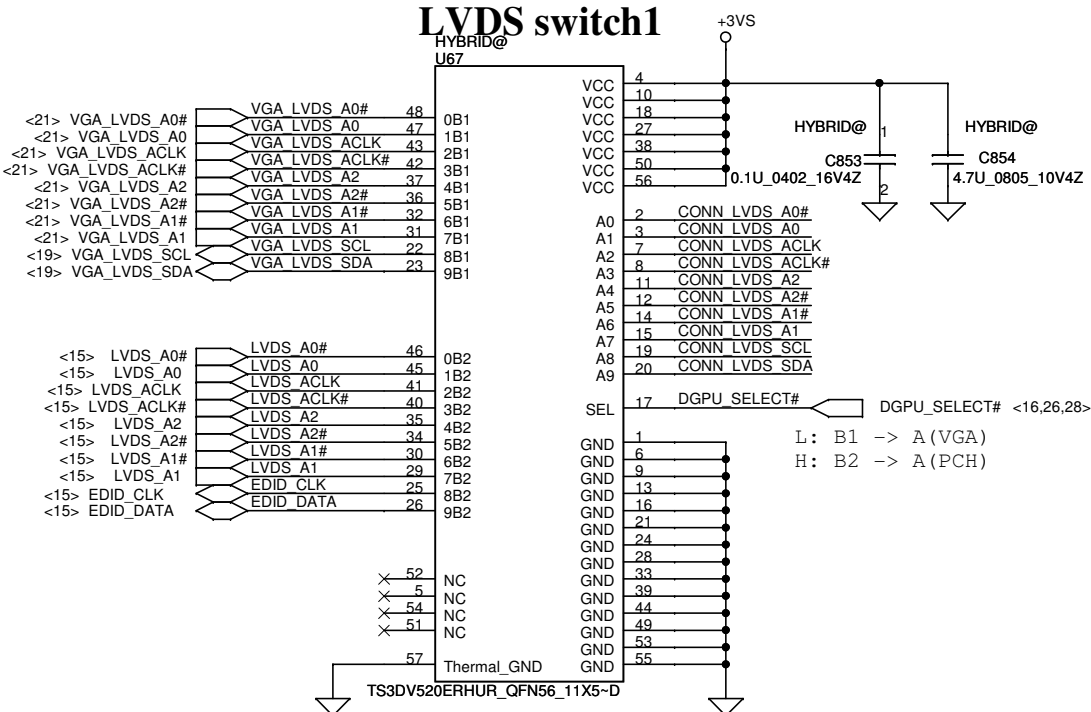
LCD POWER CIRCUIT



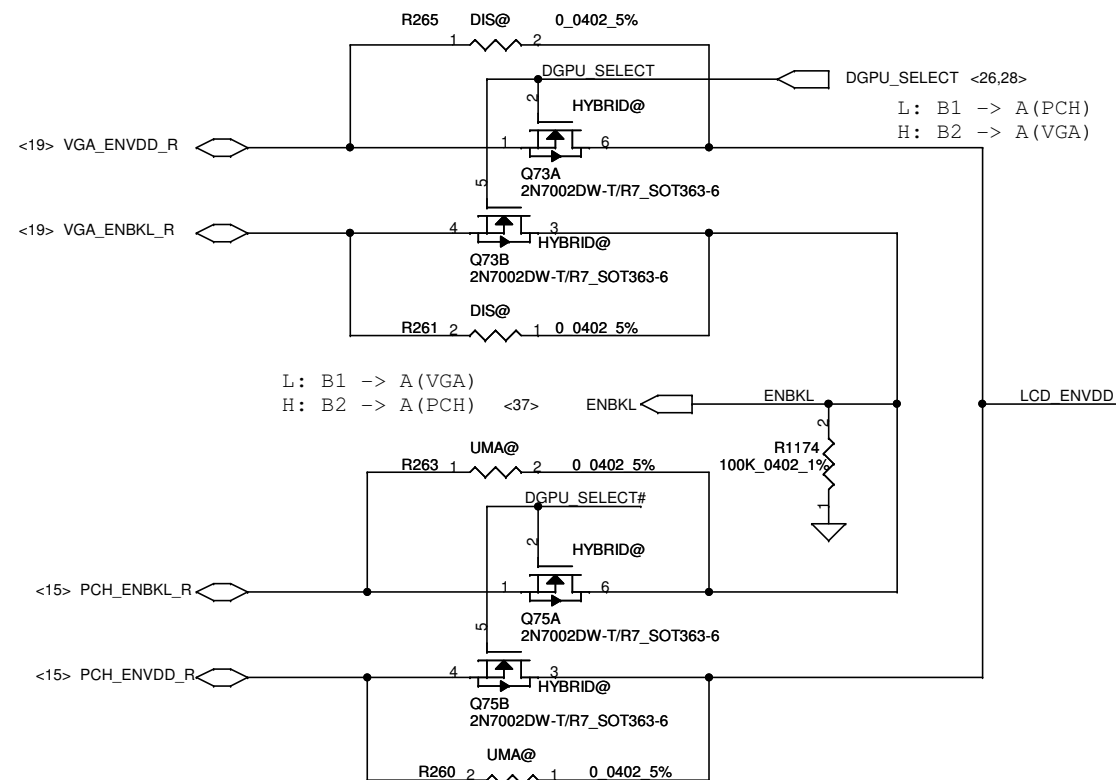
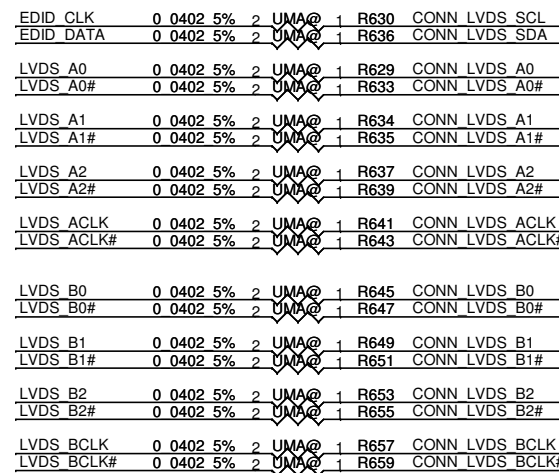
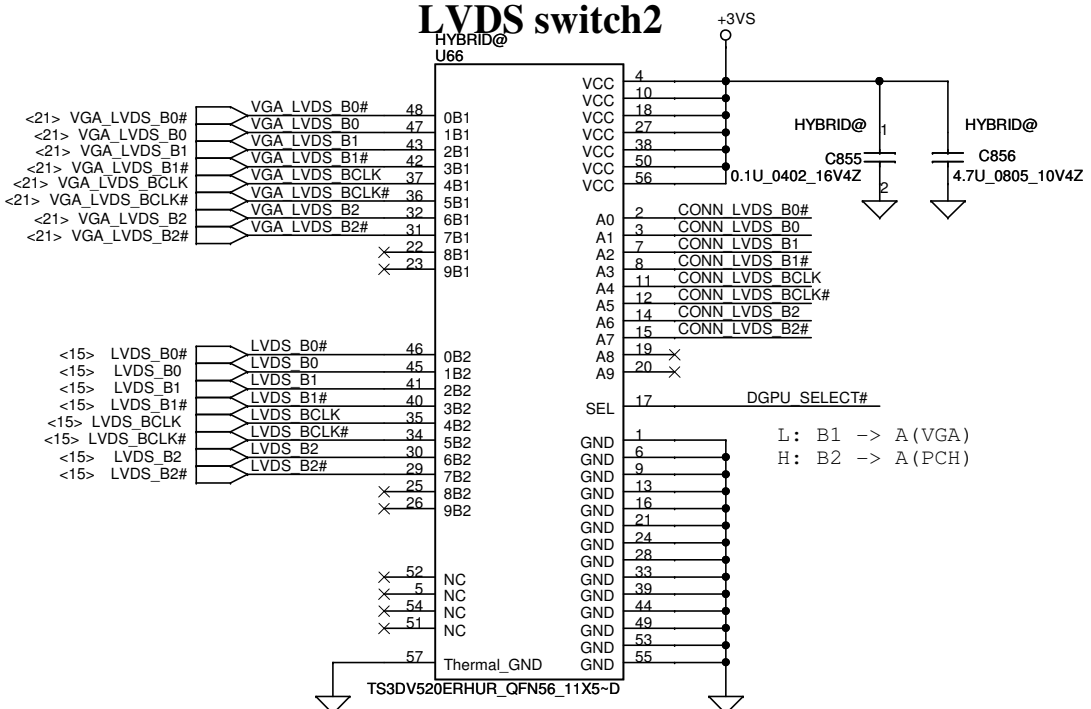
VGA LCD/PANEL BD. Conn.



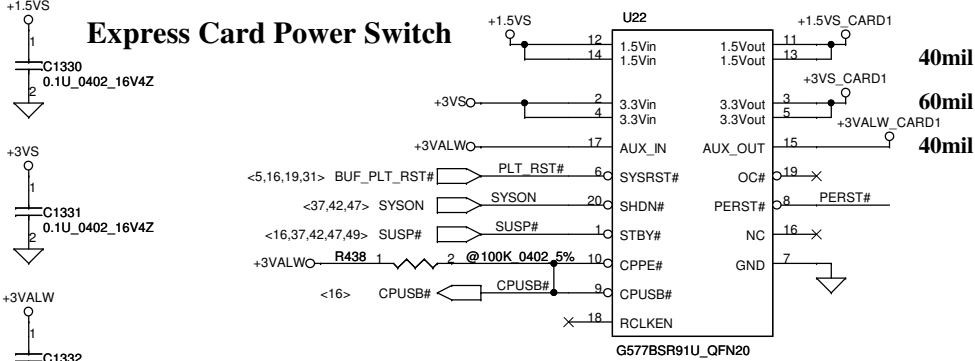
LVDS switch1



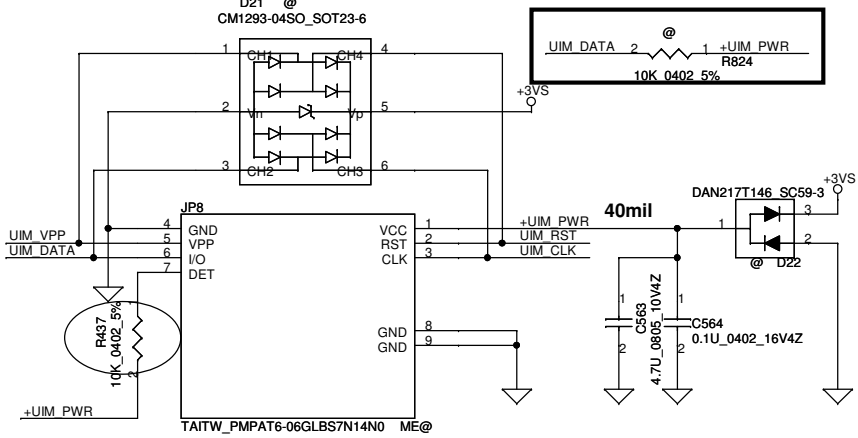
LVDS switch2



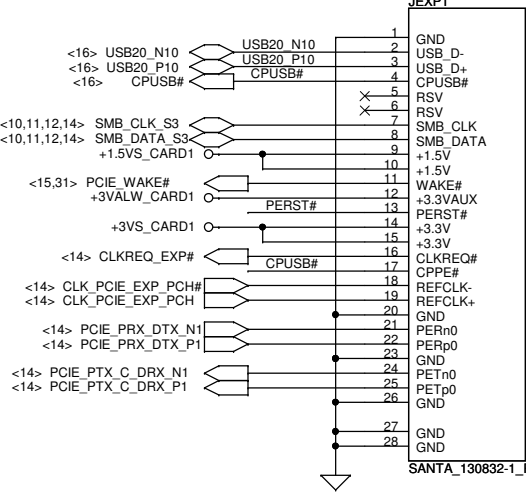
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title		
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				Size B	Document Number	Rev
				NIWBA_LA5371P		0.1
				Date	Tuesday, March 24, 2009	Sheet 29 of 52

Mini-Express Card(Slot 1-TV TUNNER) 4.0mm high

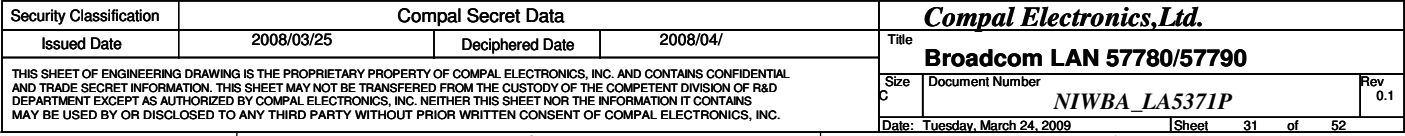
5.6mm high

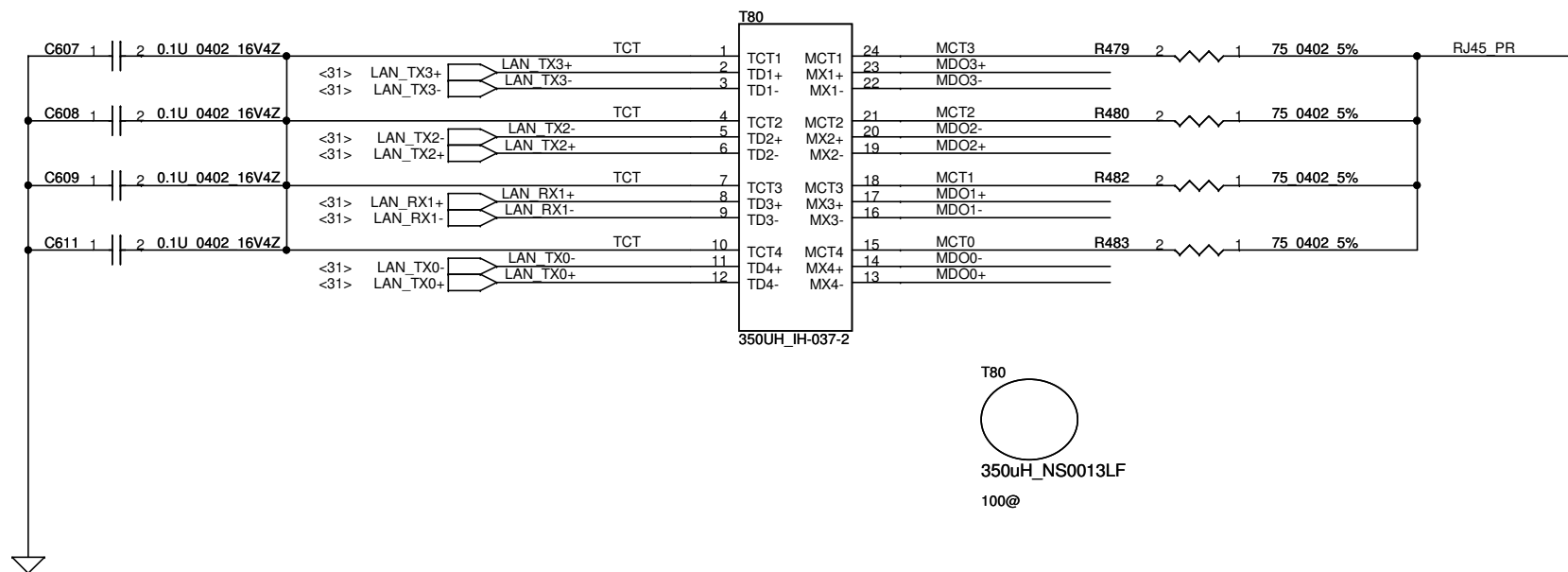


New Card 34mm Socket (Left/TOP)

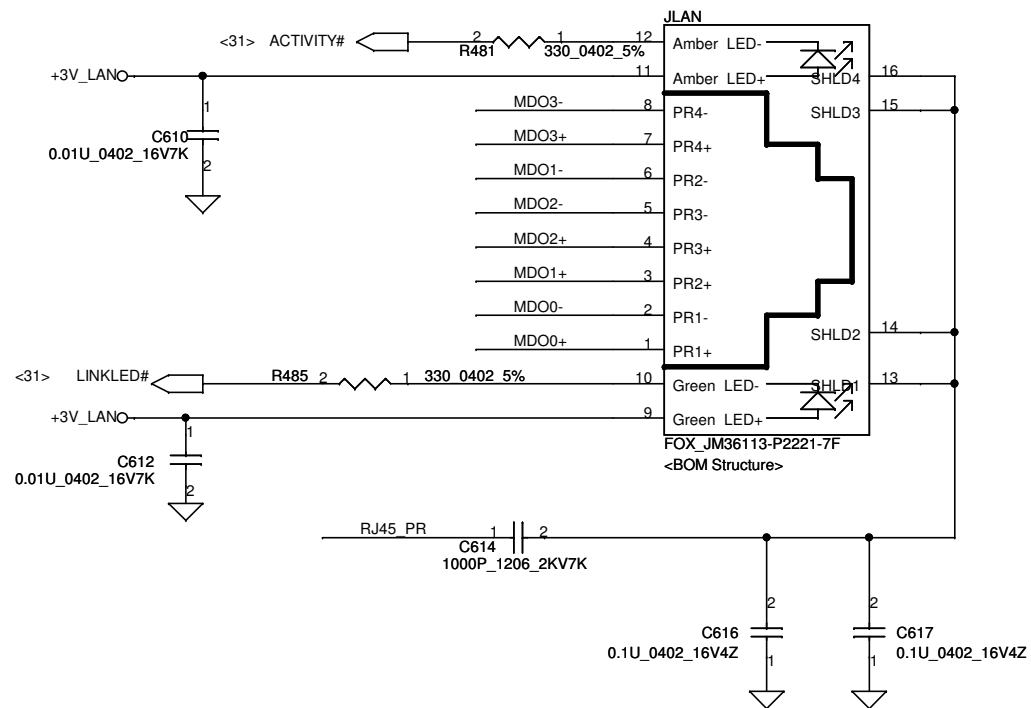


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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	Mini-Card/3G/FeliCa/BT		
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				NIWBA_LAS371P			0.1
				Date:	Tuesday, March 24, 2009	Sheet	30 of 52



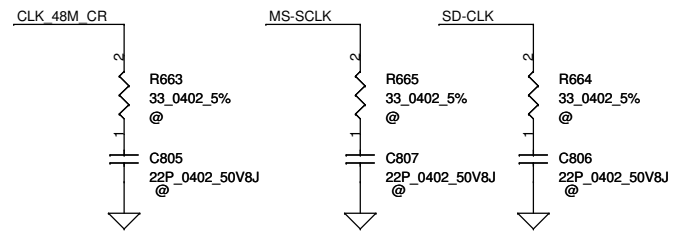
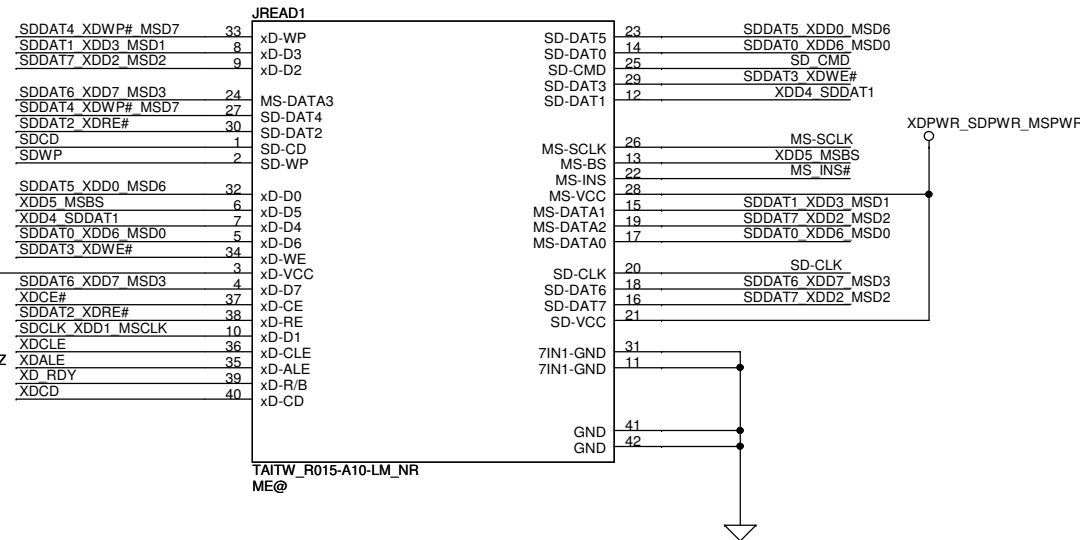
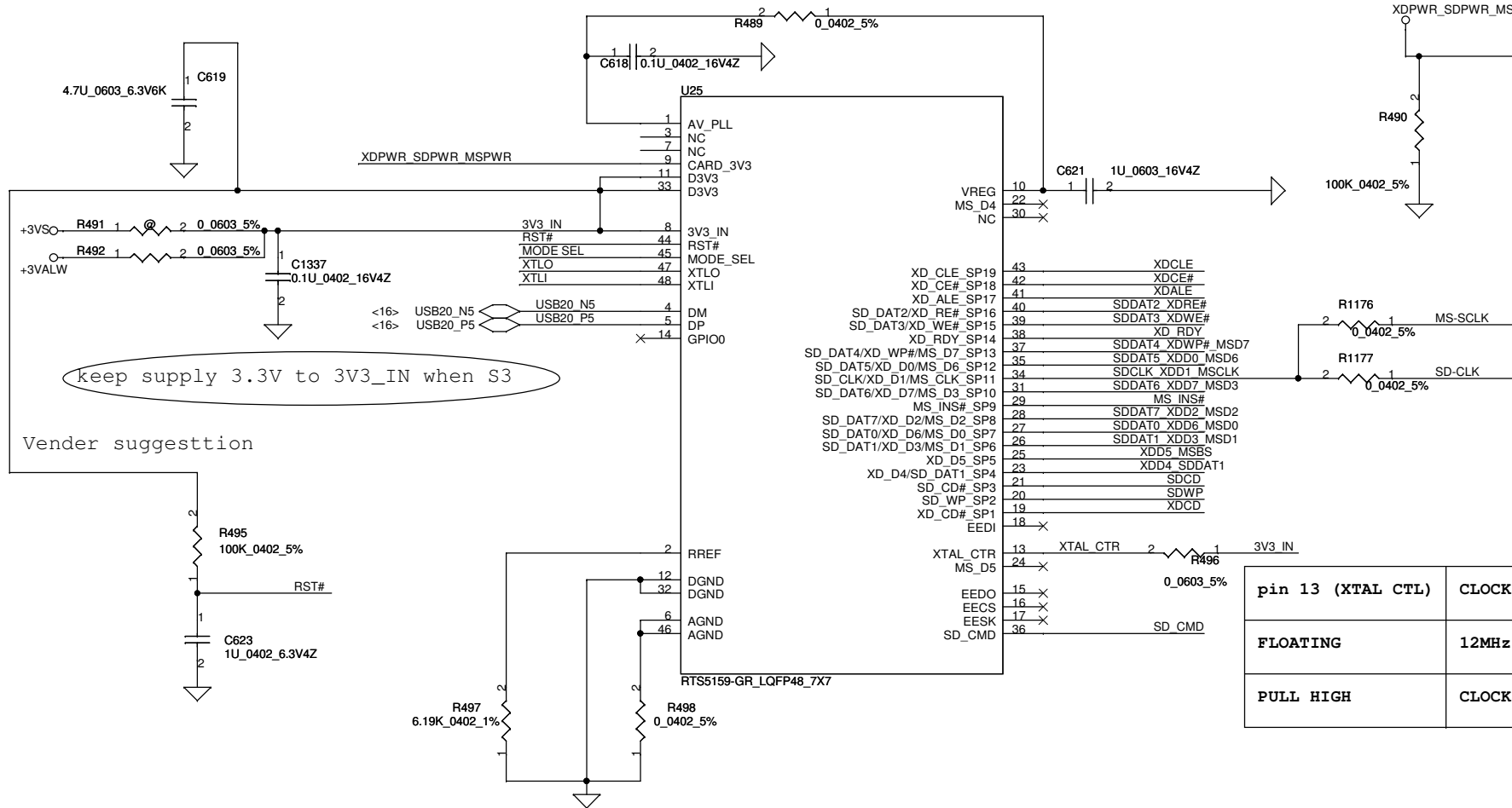


RJ11+RJ45 CONN



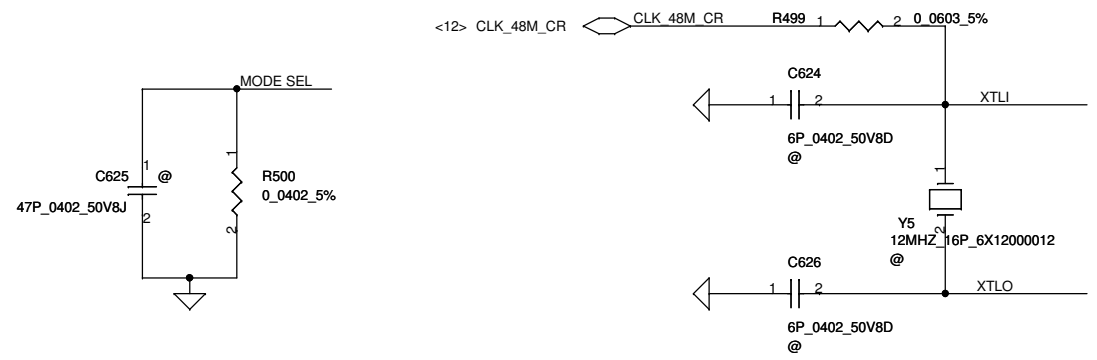
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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				Size Custom	Document Number
				KIWB1/B2_LA4601P	
Date: Tuesday, March 24, 2009		Sheet 32 of 52		Rev 0.1	

0513 : CARD_3V3 旁路電阻 100K change to 4.7u CAP==>預留
0521 : change C79 form 4.7u to 0.1u, add R47 100K ohm,
change C526 form 1u to 4.7u

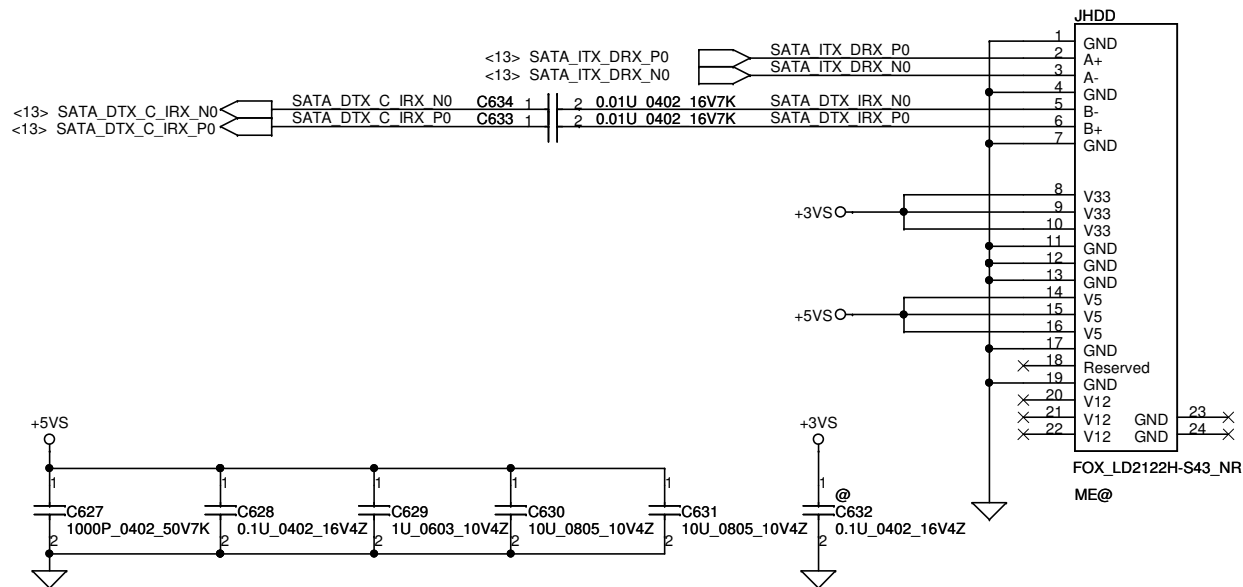


pin 13 (XTAL CTL)	CLOCK SOURCE	REMARK
FLOATING	12MHz CRYSTAL INPUT	
PULL HIGH	CLOCK GENERATOR'S 48MHZ INPUT	INPUT TO PIN48

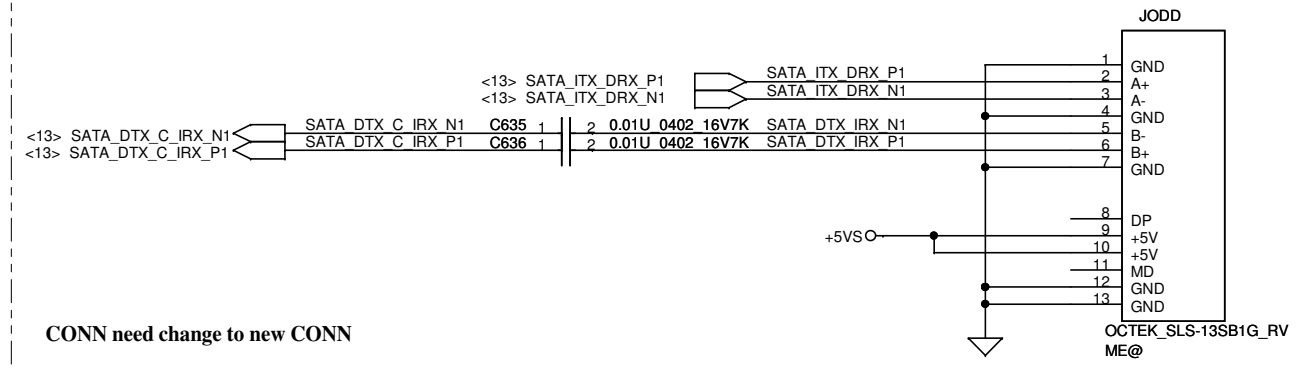
MCLK and SDCLK 該二電阻是預留給EMI solution使用, (但請靠近RTS5158E側).
將SD_DAT1 連接到RTS5158E的pin23



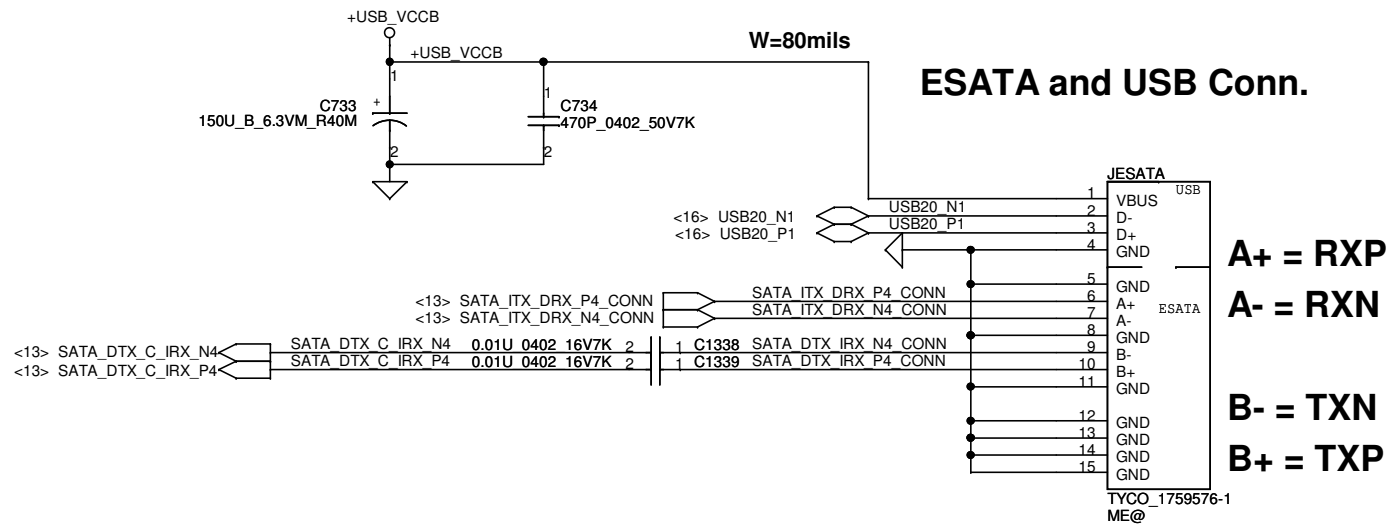
SATA HDD Conn.



SATA ODD Conn.



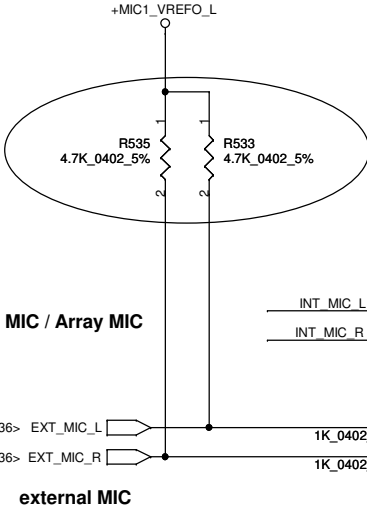
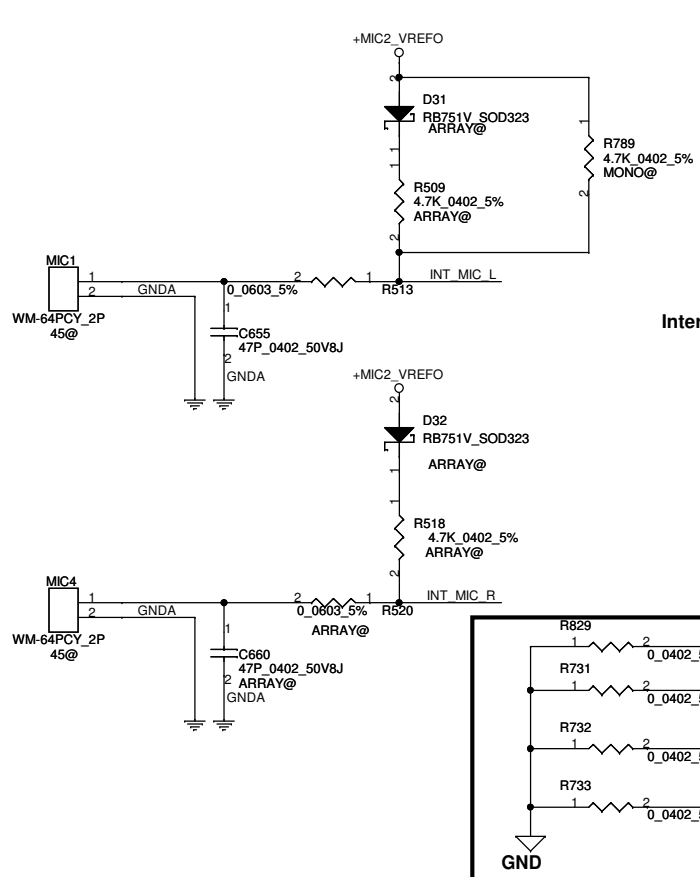
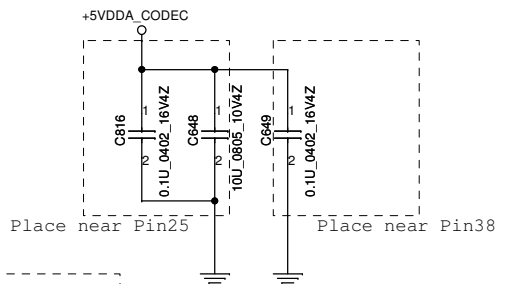
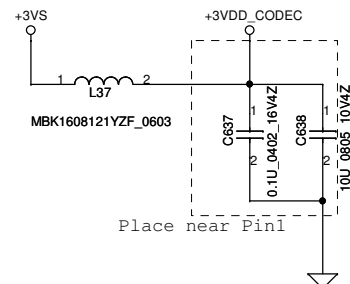
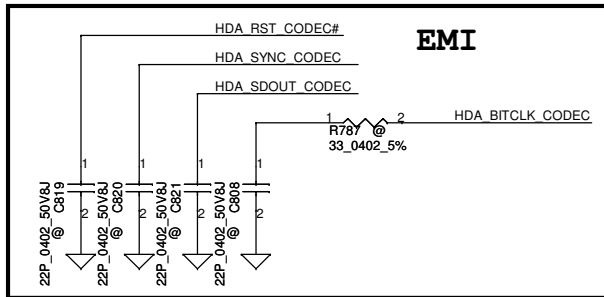
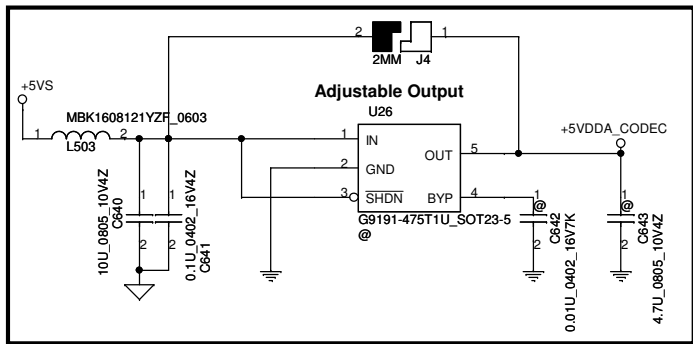
ESATA and USB Conn.



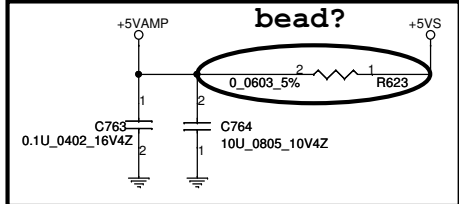
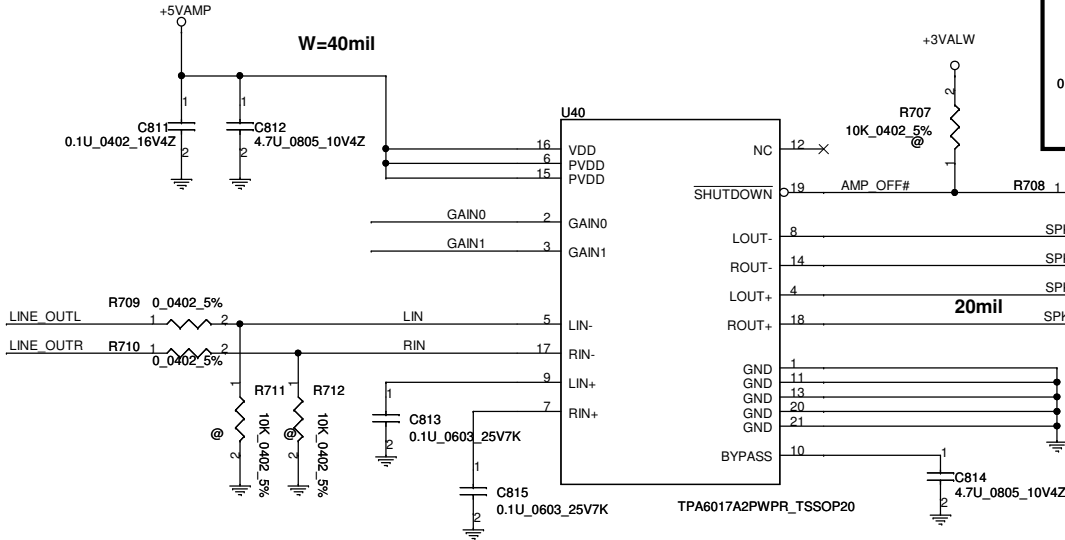
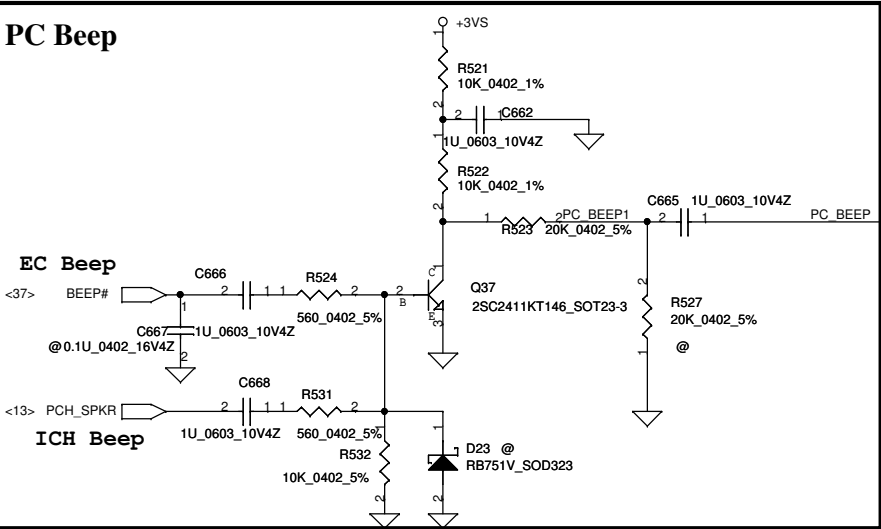
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A- = RXN

B- = TXN
B+ = TXP

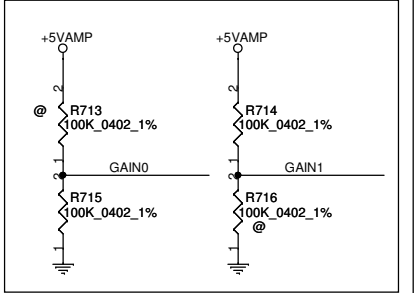
Security Classification	Compal Secret Data			Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	HDD & ODD Connector	
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Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1 (Pin21/22)	External	Mic in
MONO-OUT (Pin37)	Internal	Internal Subwoofer
MIC2 (Pin16/17)	Internal	Internal Mic

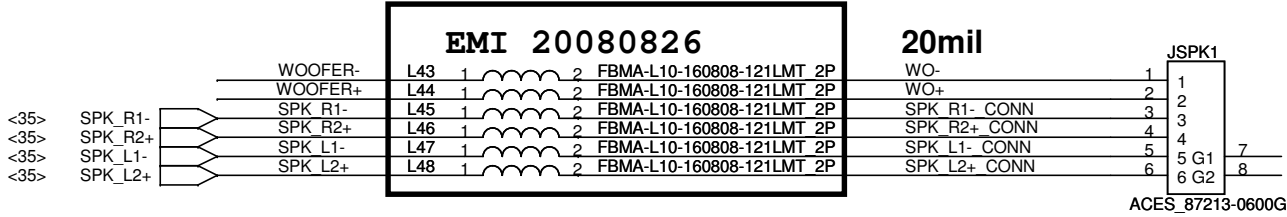


GAIN0	GAIN1	Gain
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



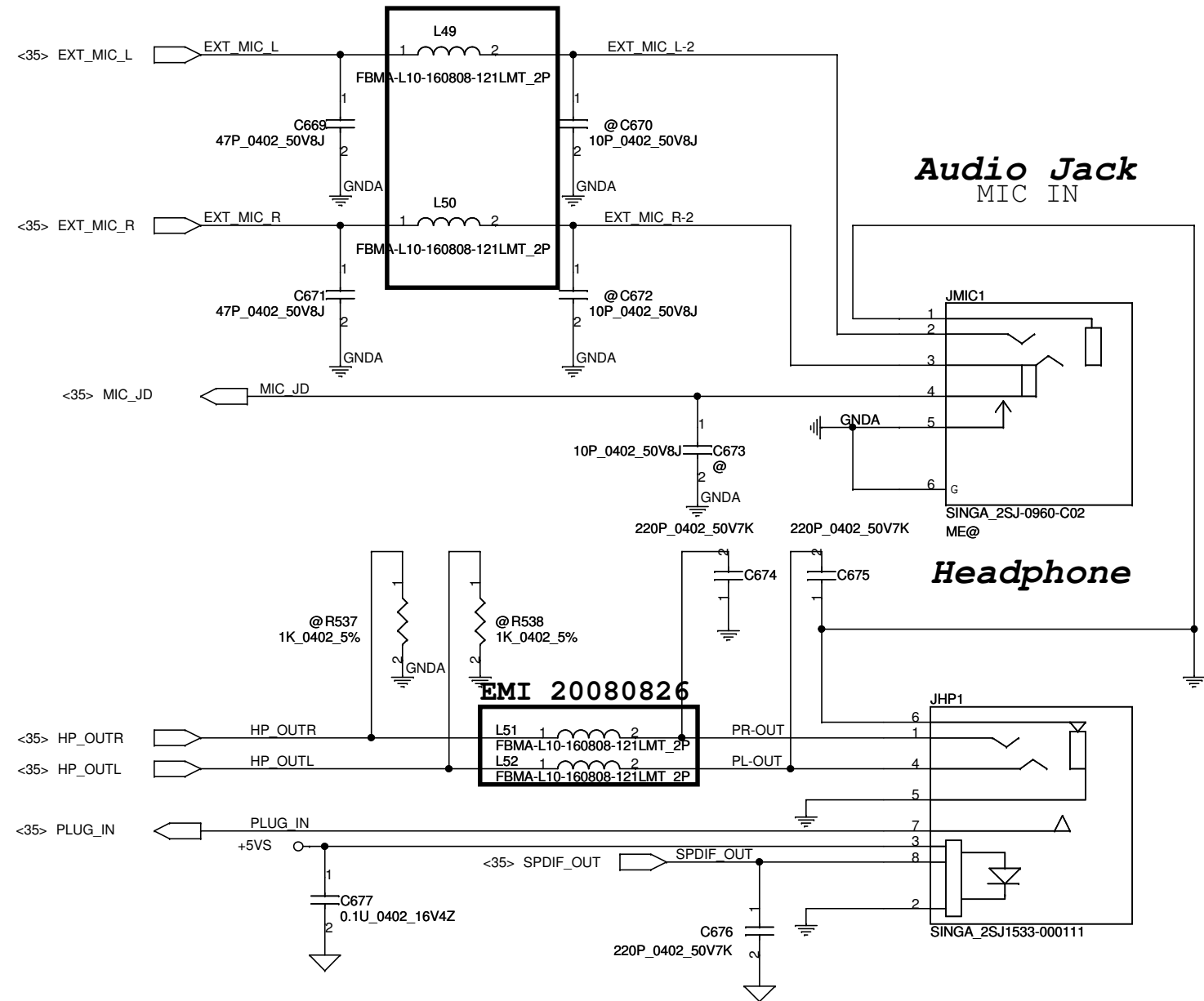
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Size	Document Number	Rev	NIWBA_LA5371P	
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SubWoofer Conn. Speaker Connector



Audio Jack

EMI 20080826

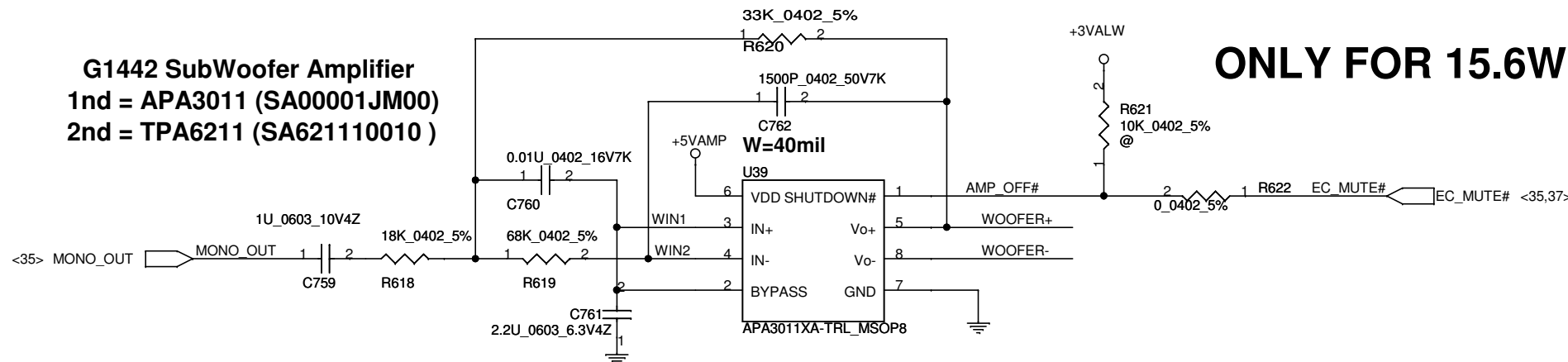


Audio Jack MIC IN

Headphone

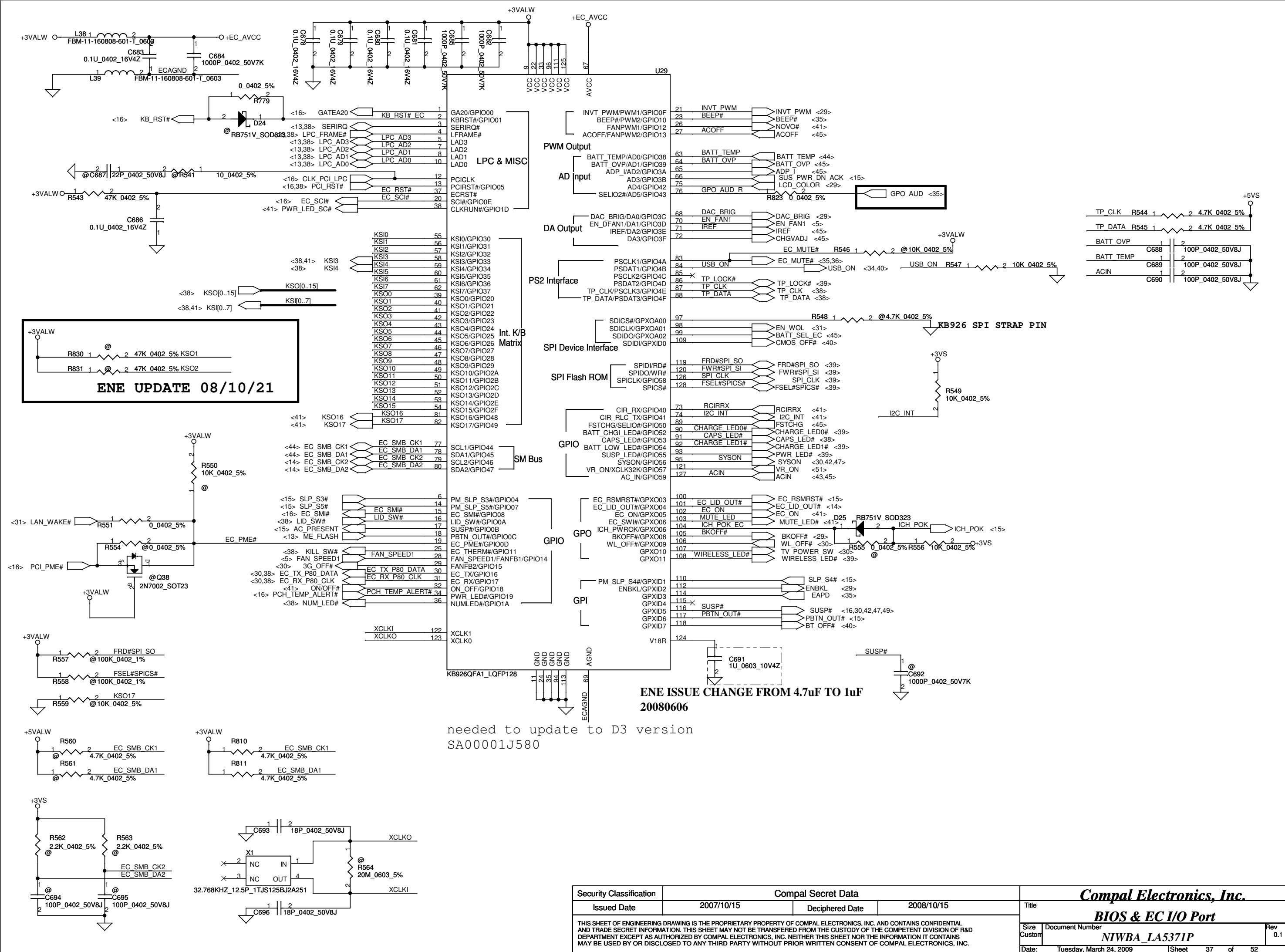
G1442 SubWoofer Amplifier

1nd = APA3011 (SA00001JM00)
2nd = TPA6211 (SA621110010)

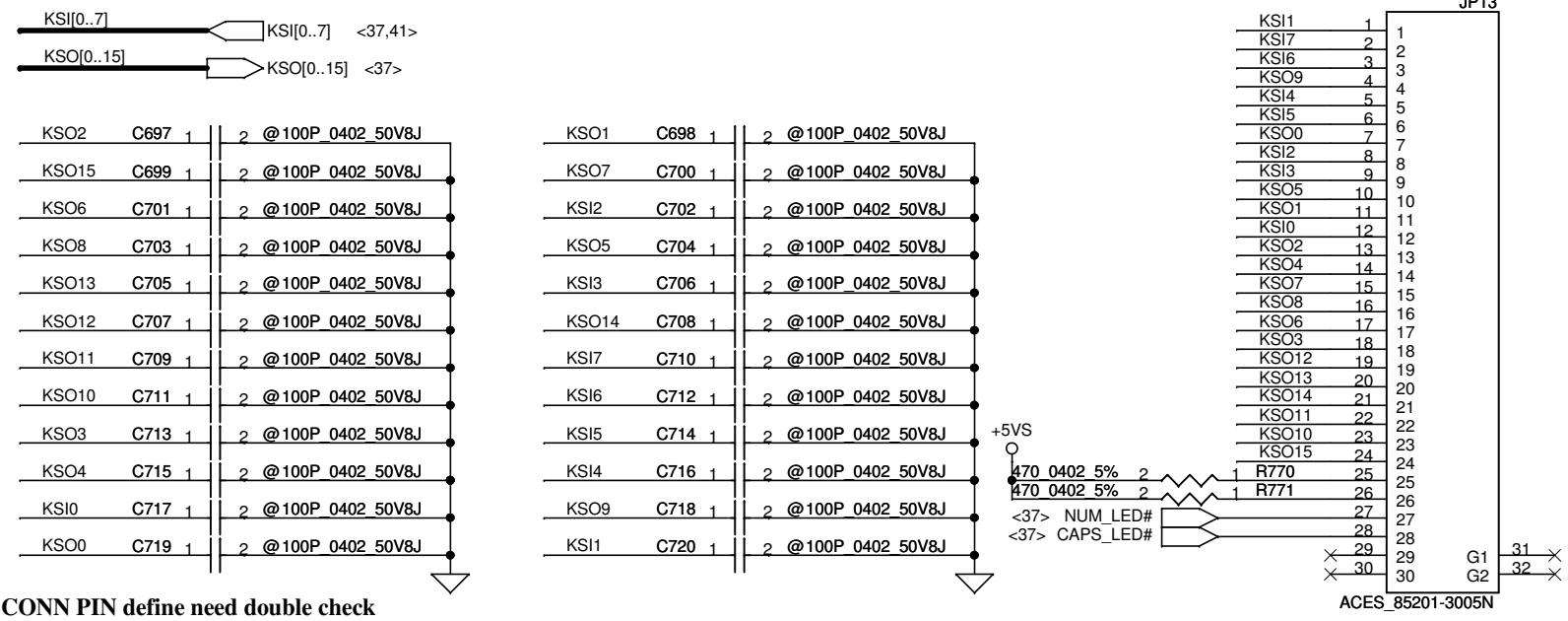


ONLY FOR 15.6W

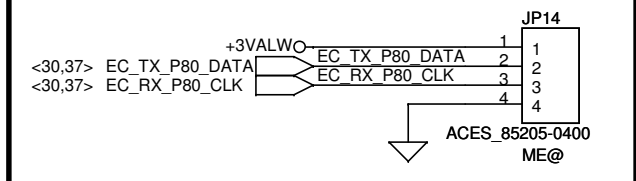
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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title AMP, Audio speaker CONN	
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				Date: Tuesday, March 24, 2009	Rev 0.1
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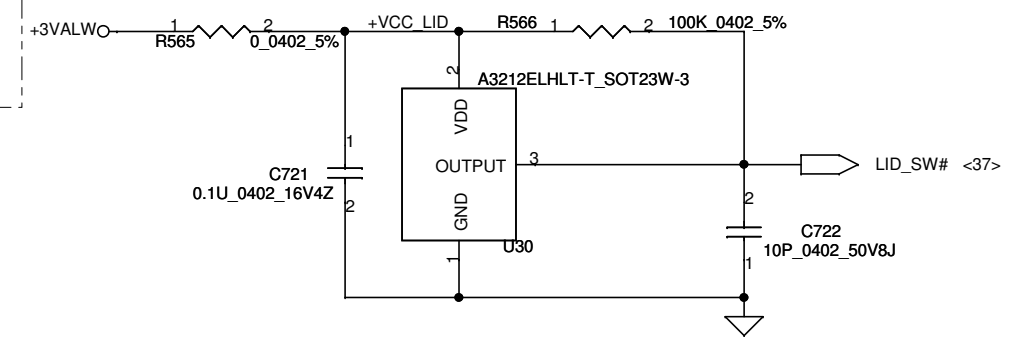
INT_KBD Conn.



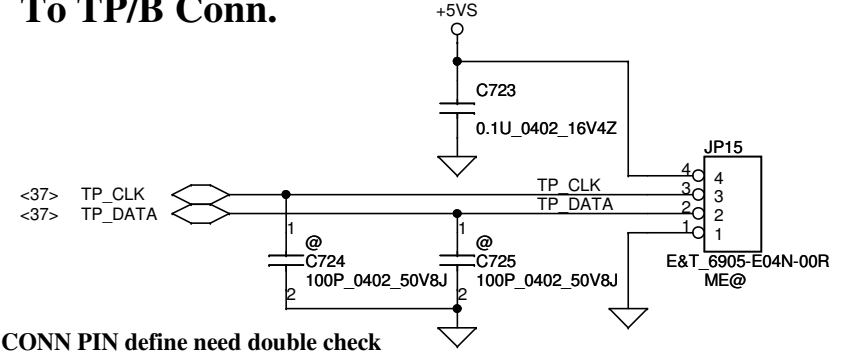
EC DEBUG PORT



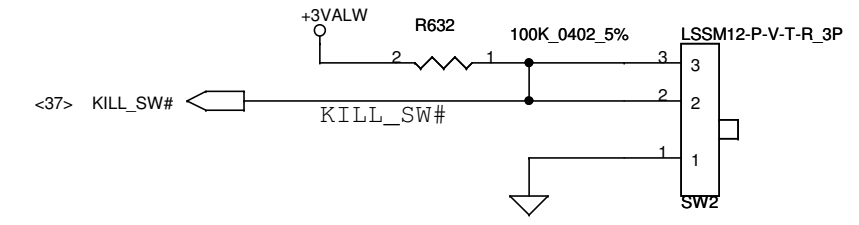
Lid Switch



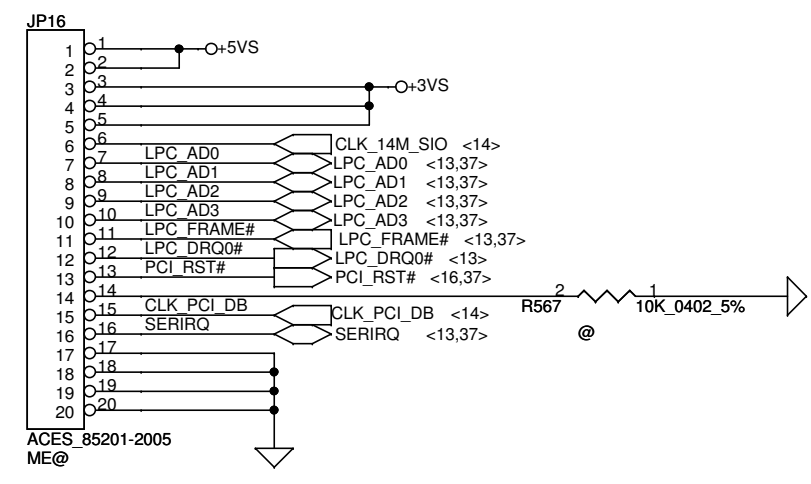
To TP/B Conn.



Kill Switch

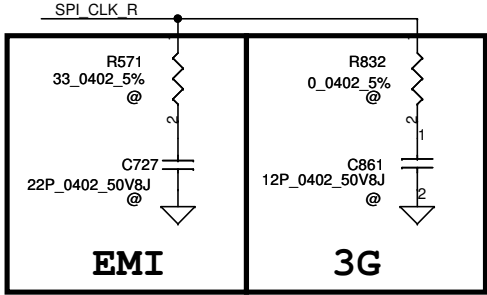
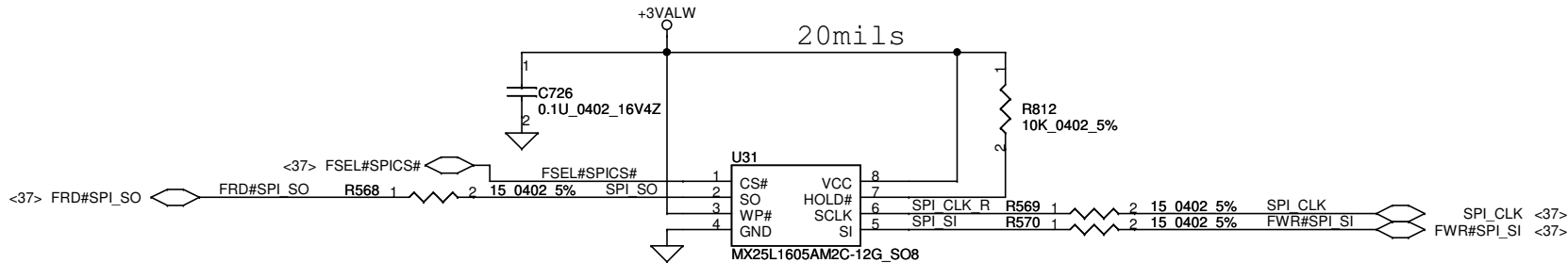


FOR LPC SIO DEBUG PORT



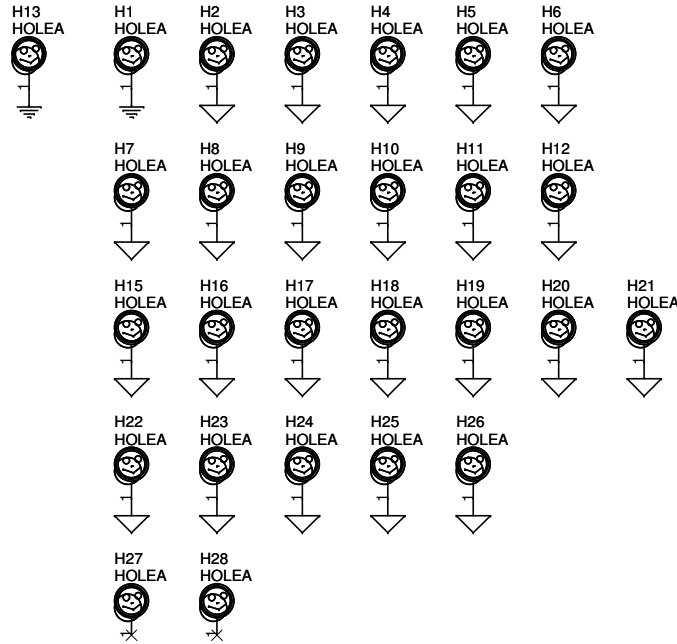
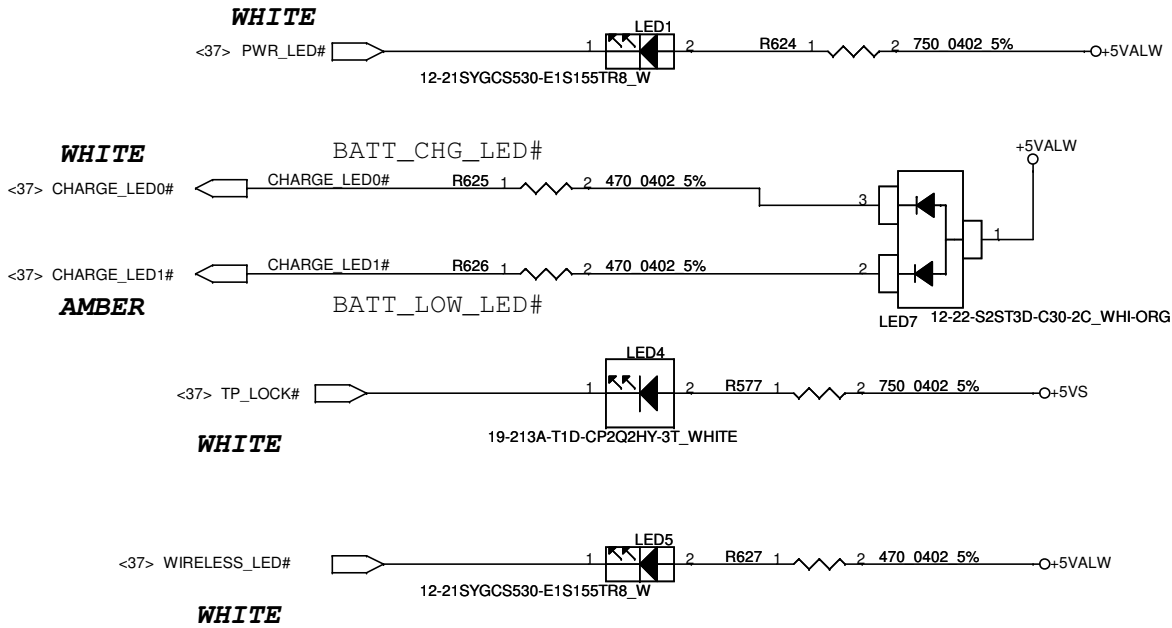
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Issued Date		2007/10/15		Deciphered Date		2008/10/15		Title			
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						Size	Document Number			Rev	
							KIWB1/B2_LA4601P			0.1	
Date:		Tuesday, March 24, 2009		Sheet		38		of		52	
3		2		1							

FOR EC 16M SPI ROM

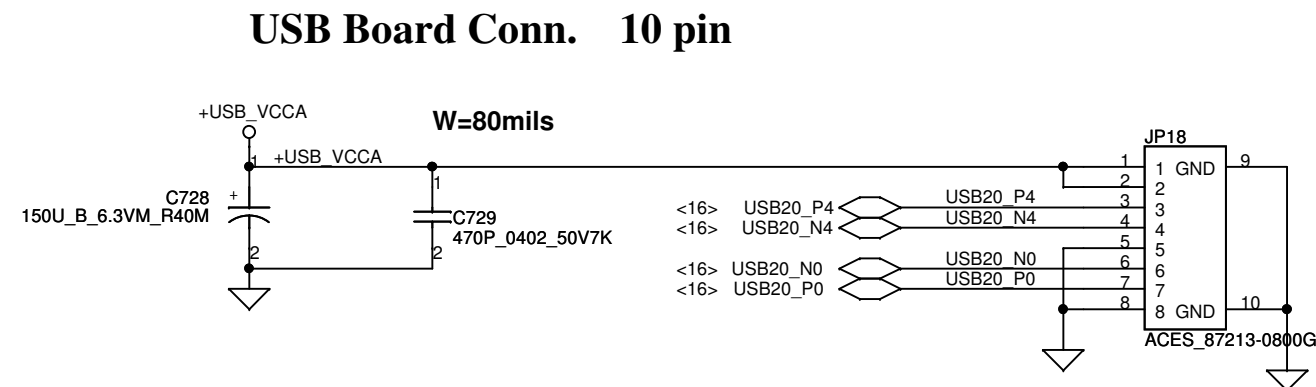
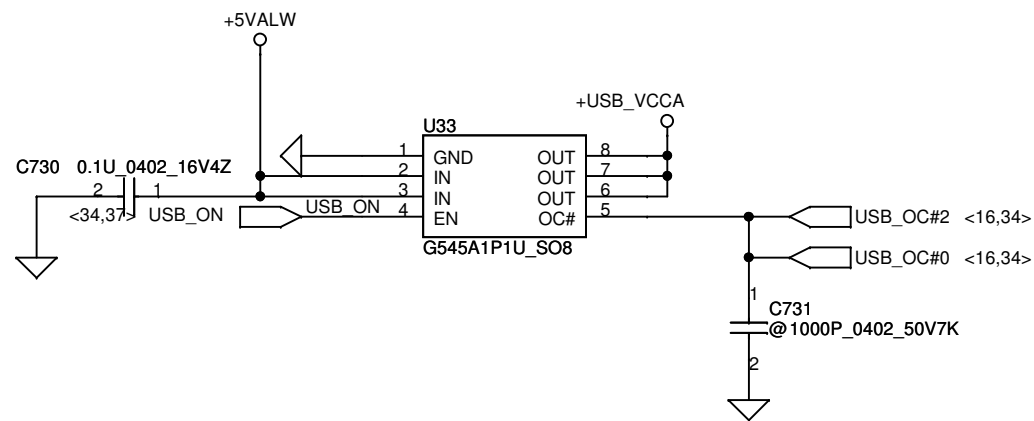


LED

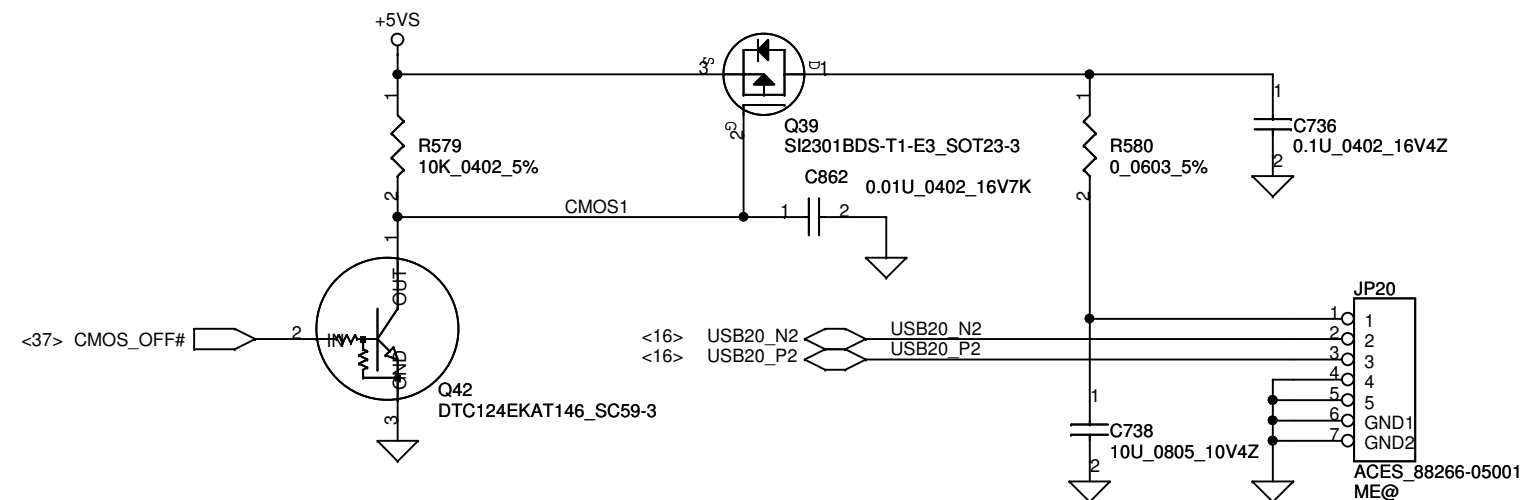
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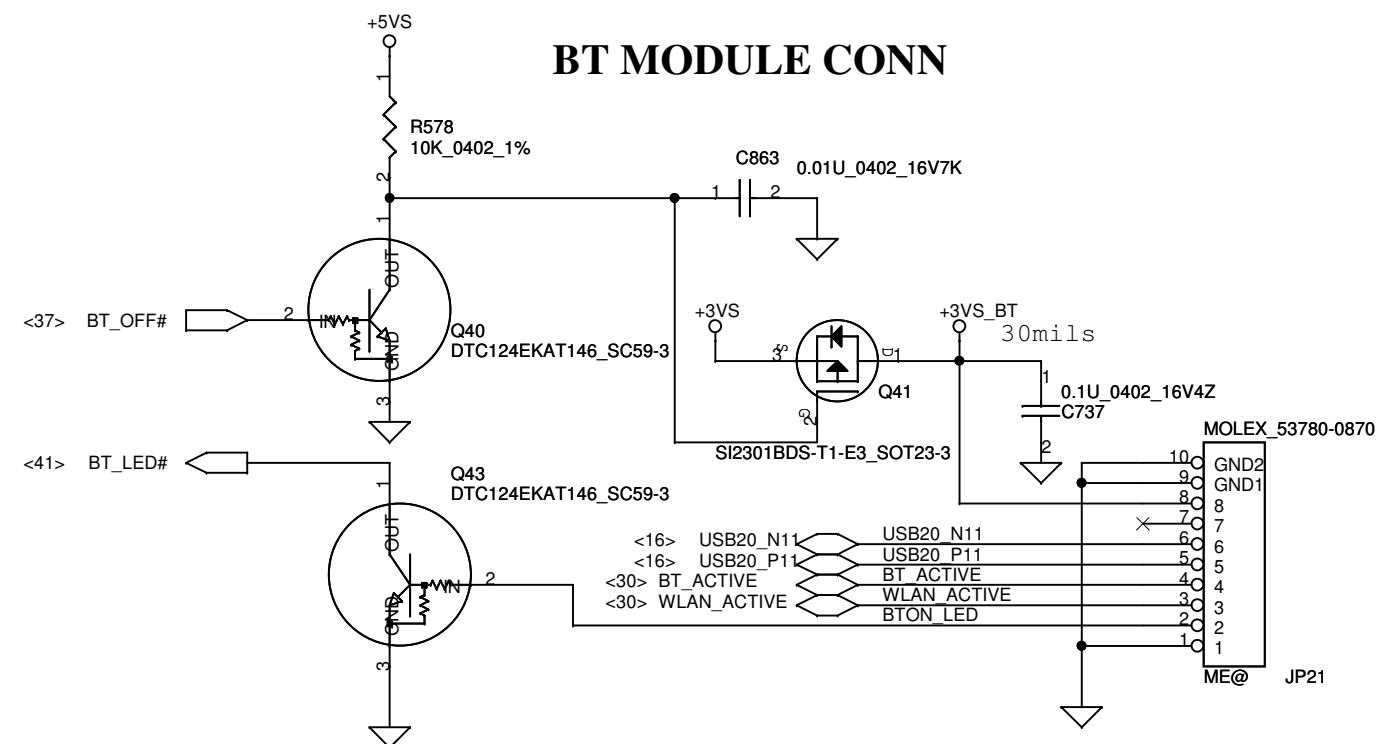
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				Document Number	
				NIWBA_LA5371P	
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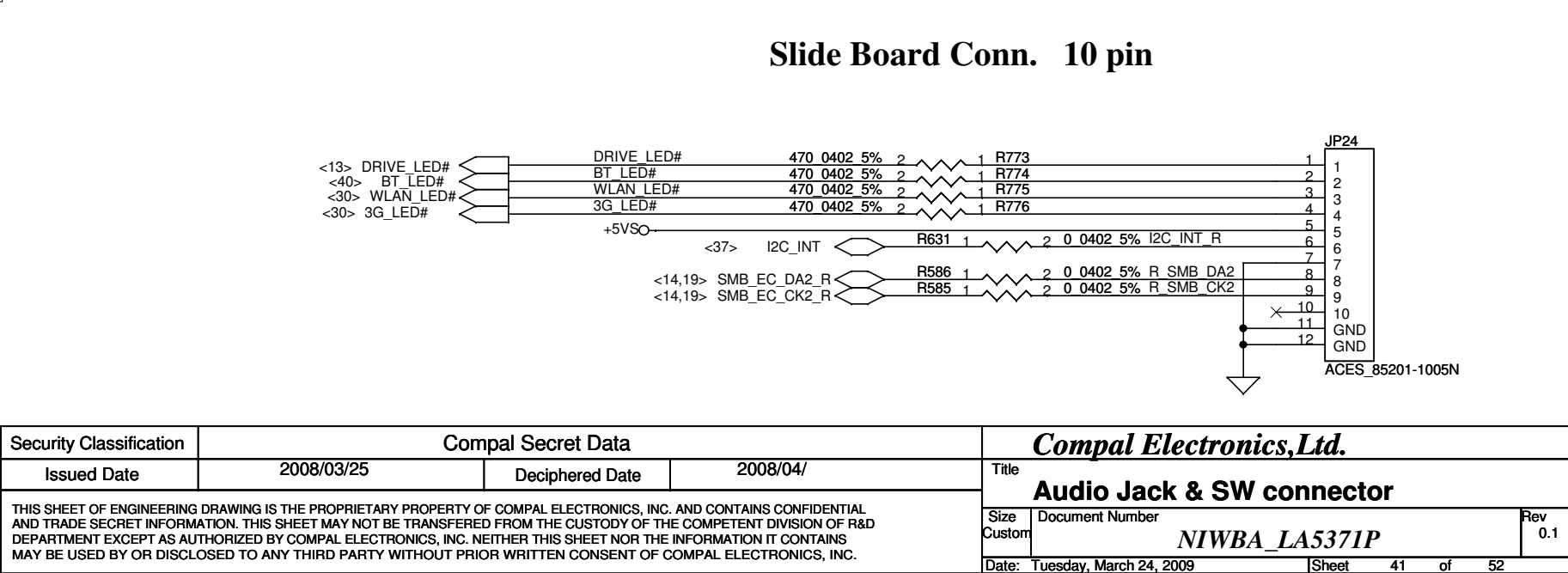
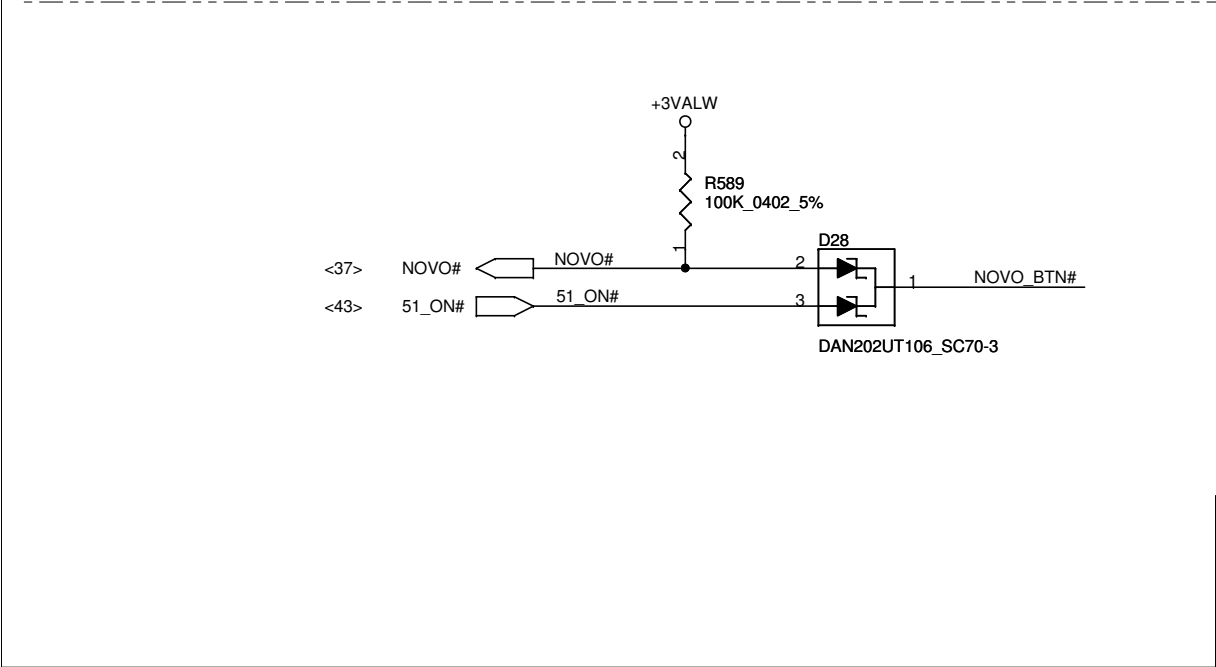
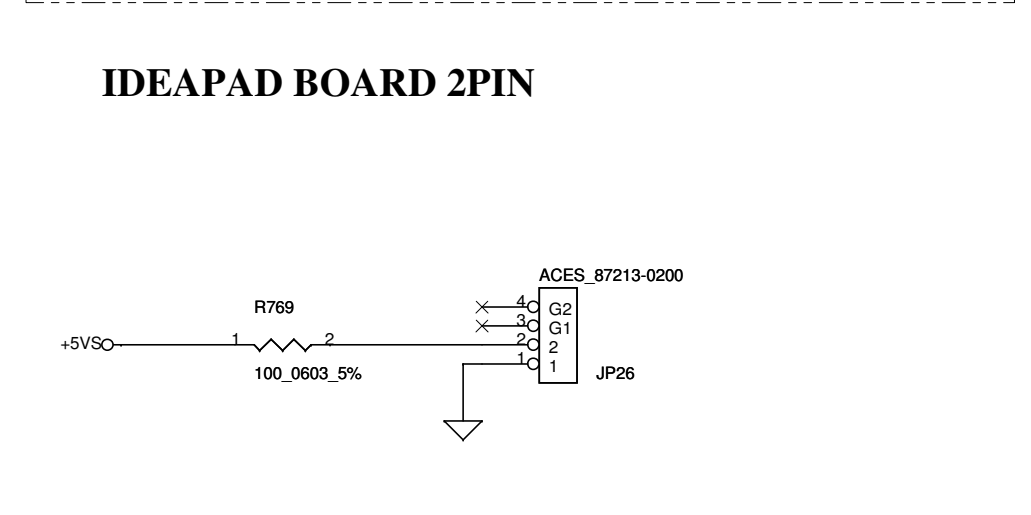
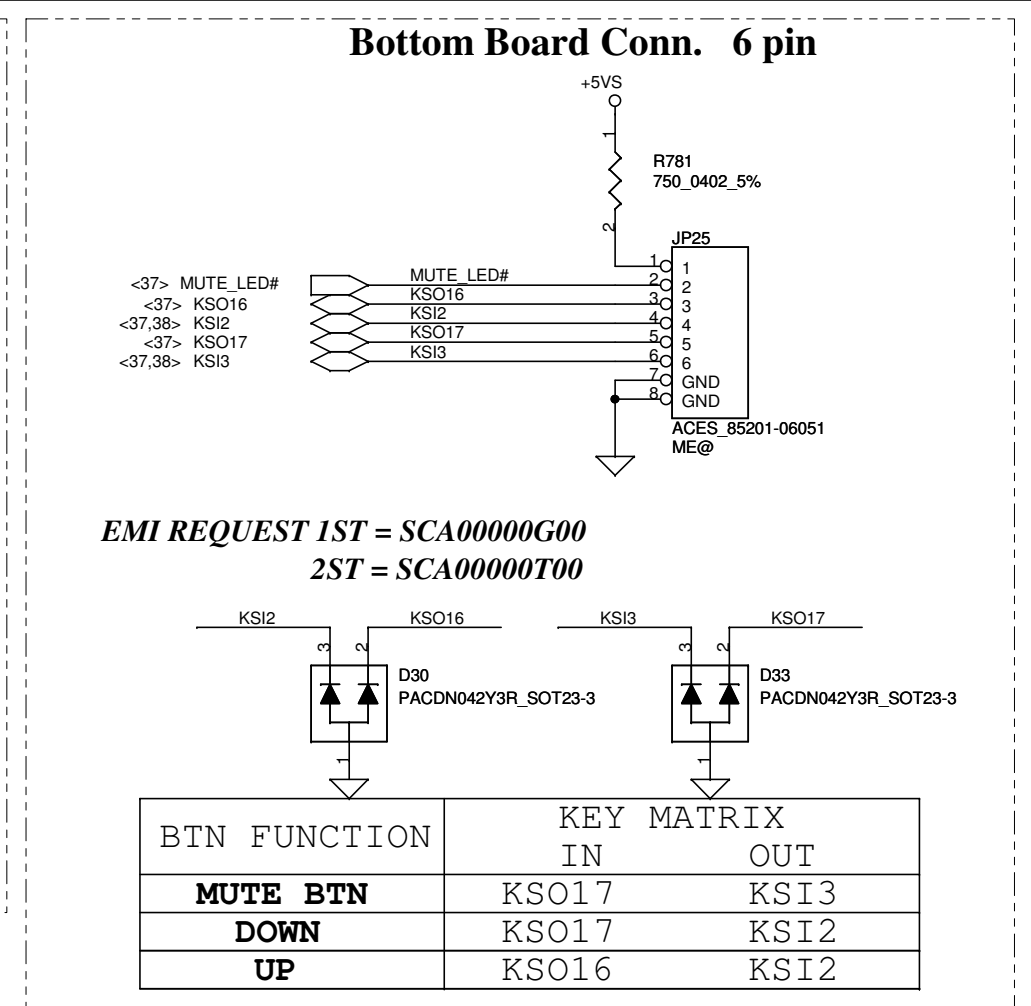
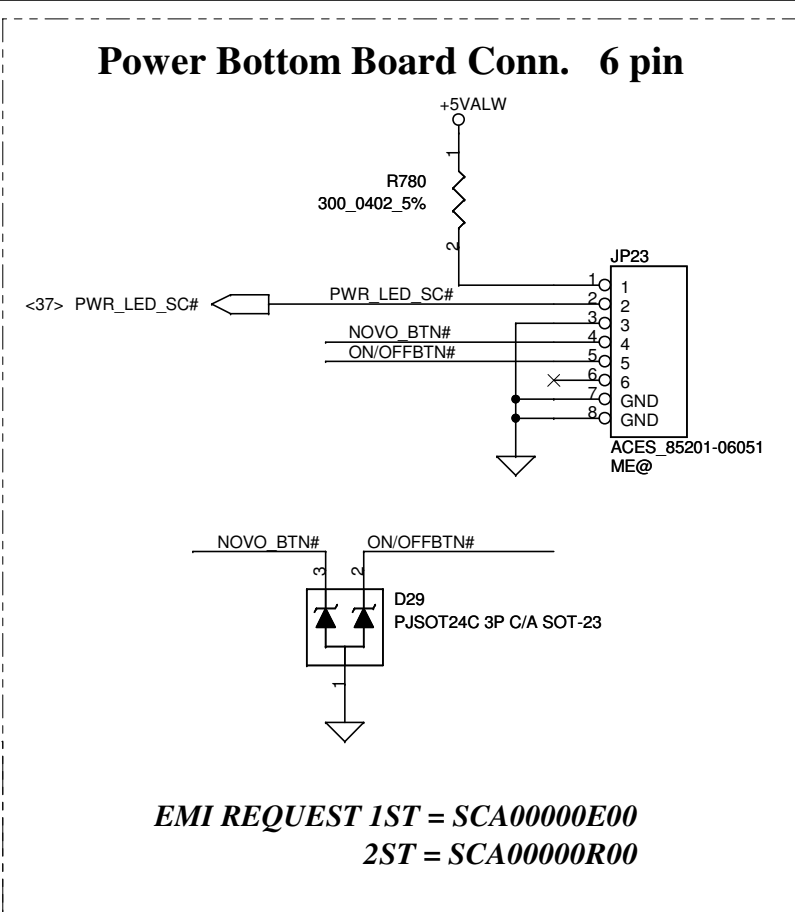
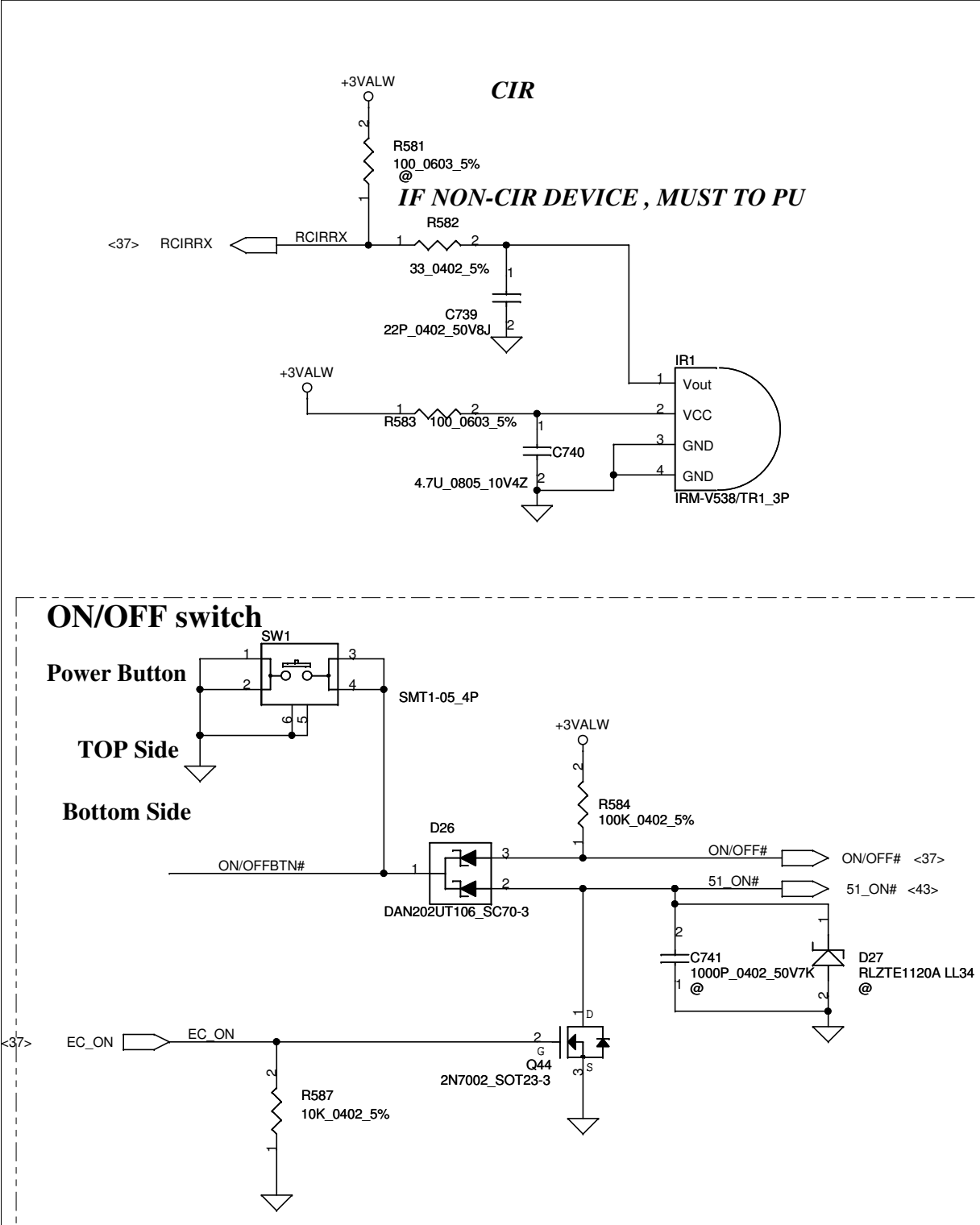
CMOS Camera Conn

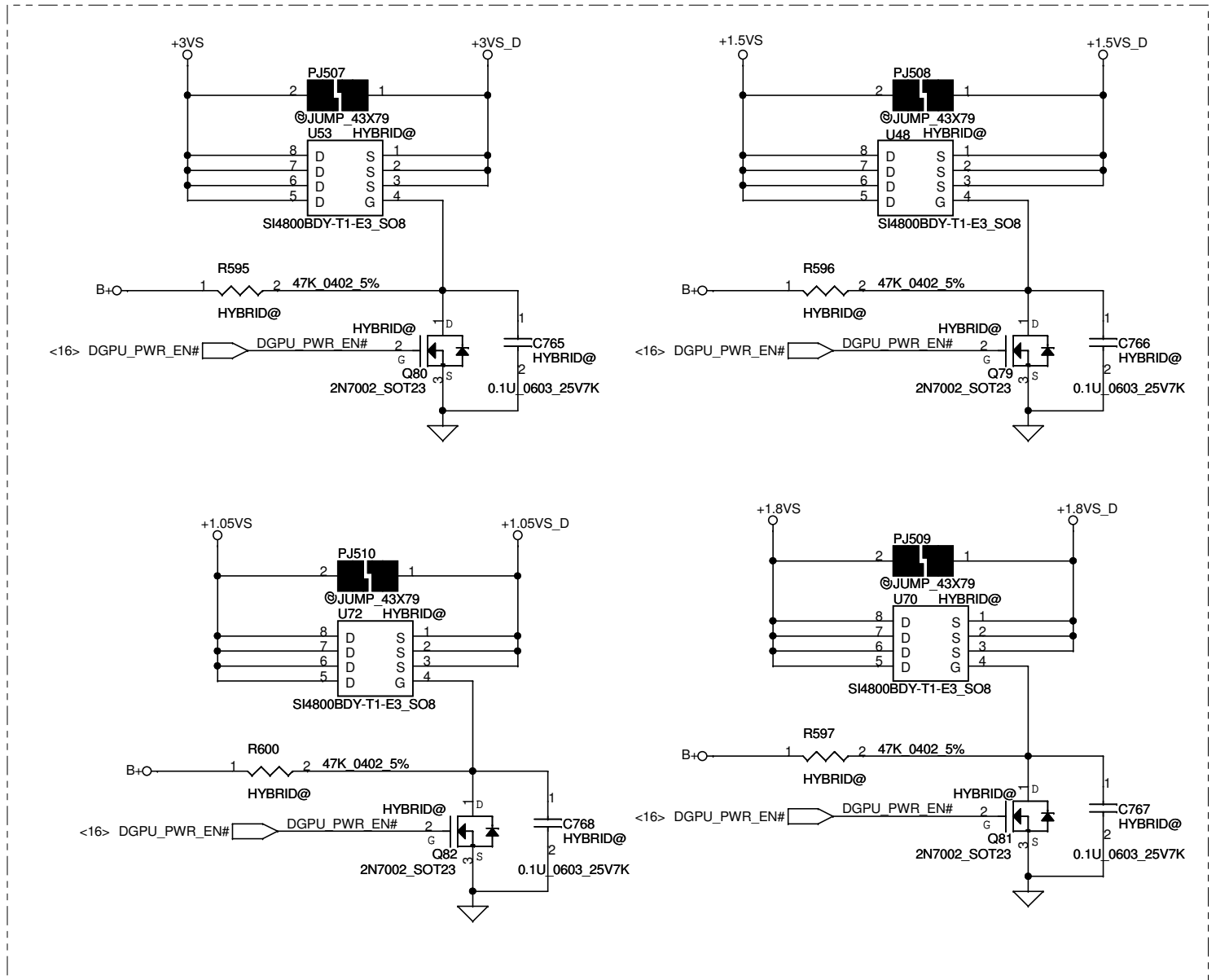
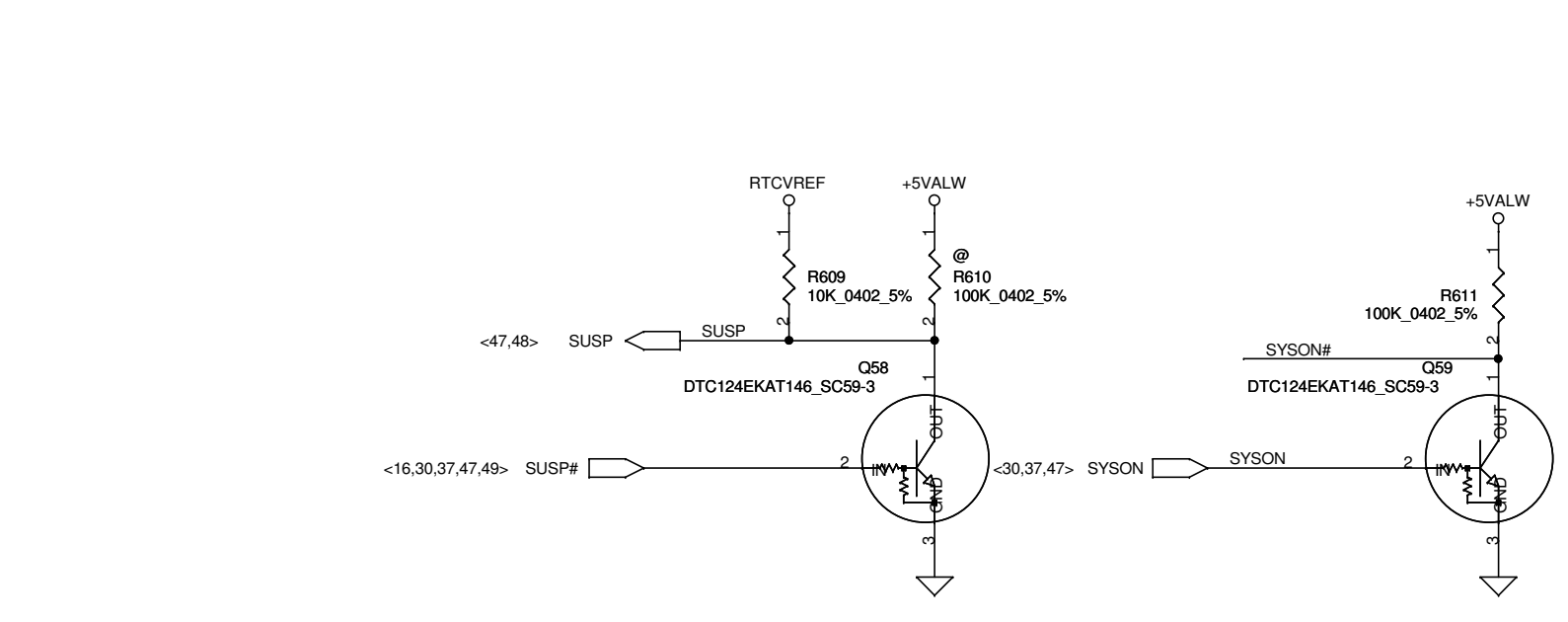
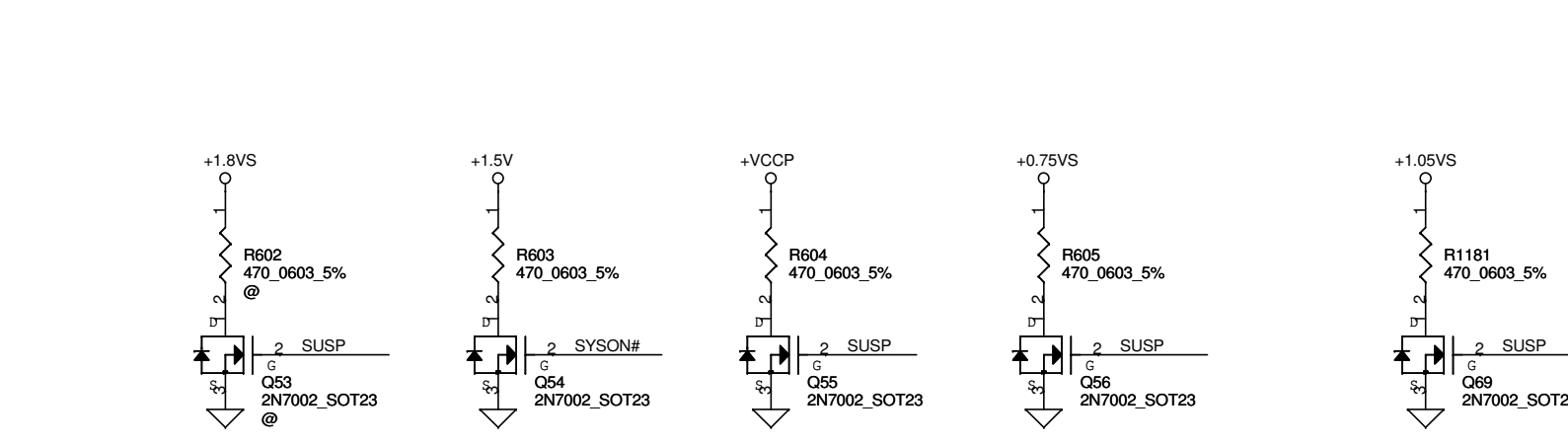
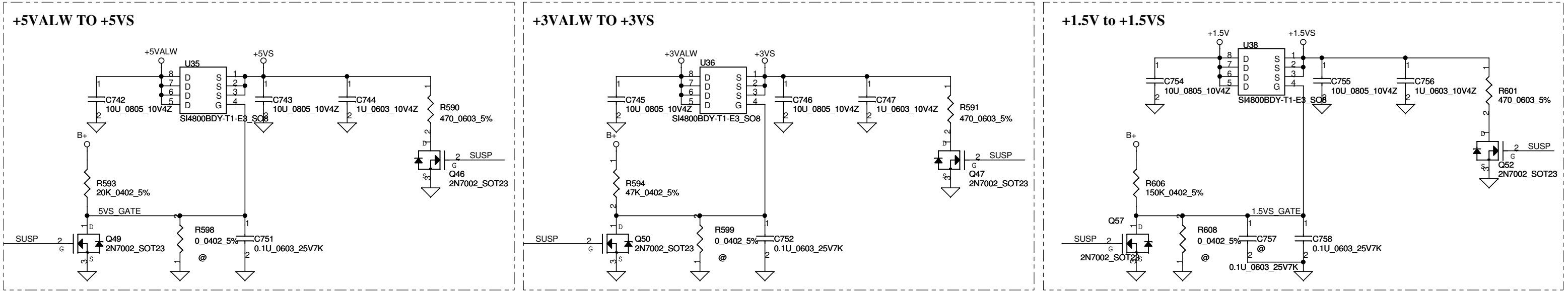


BT MODULE CONN



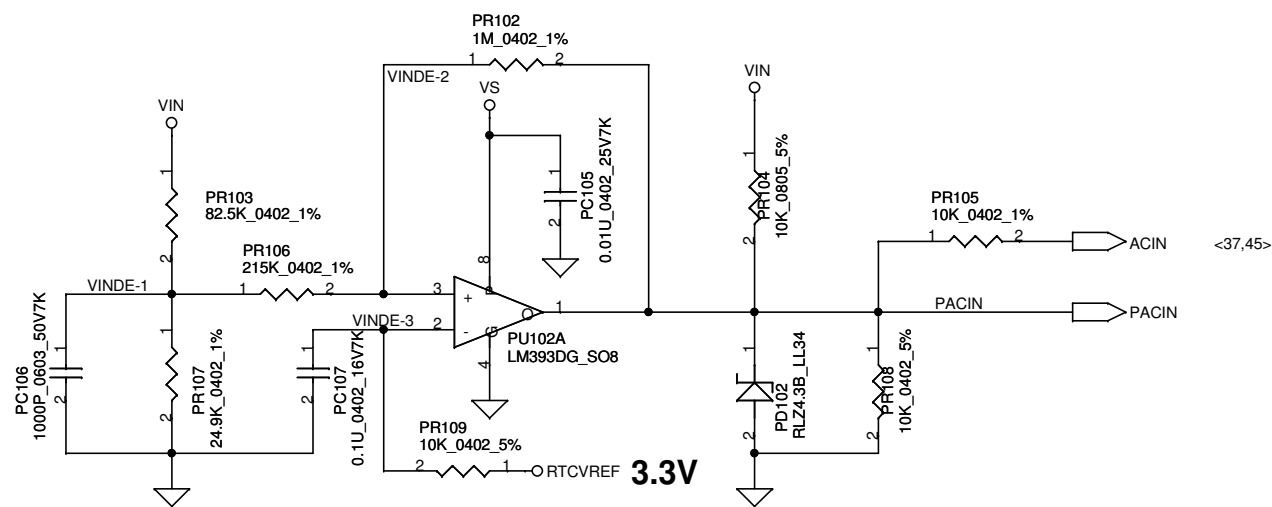
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				Size Custom Document Number NIWBA_LA5371P Rev 0.1
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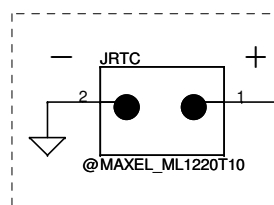


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				Size	Document Number
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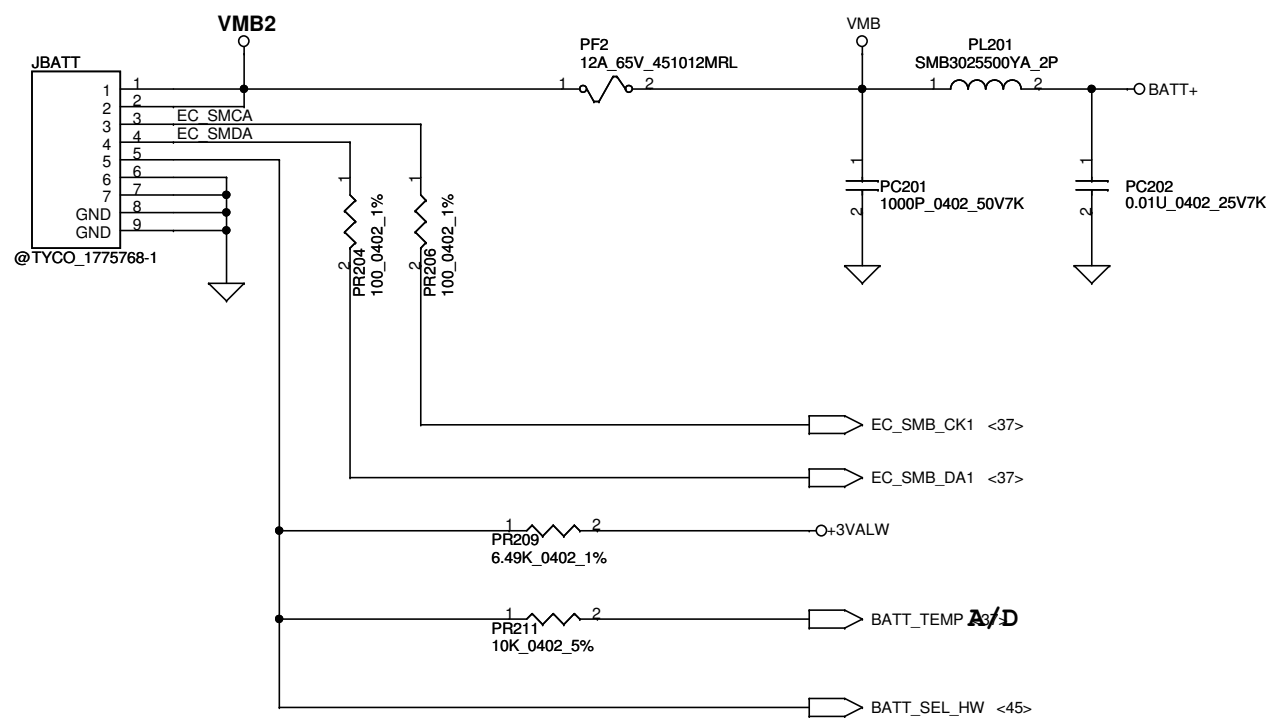
JDCIN
@4602-Q04C-09R 4P P2.5



High	18.135	17.566	17.011
Low	14.866	14.355	14.063



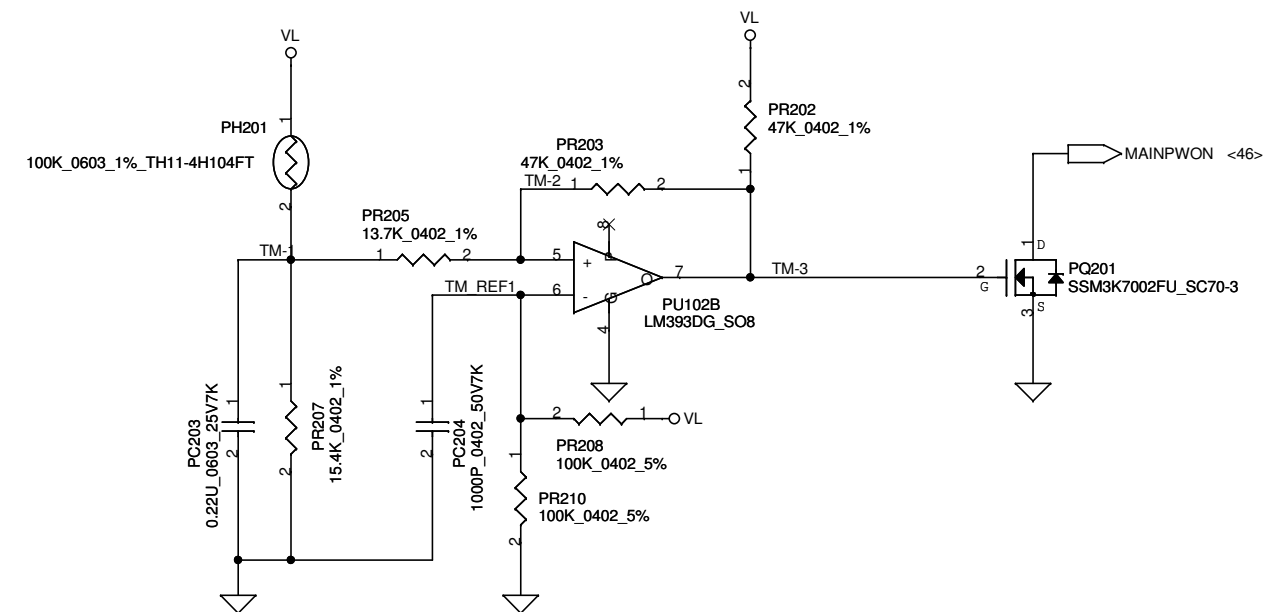
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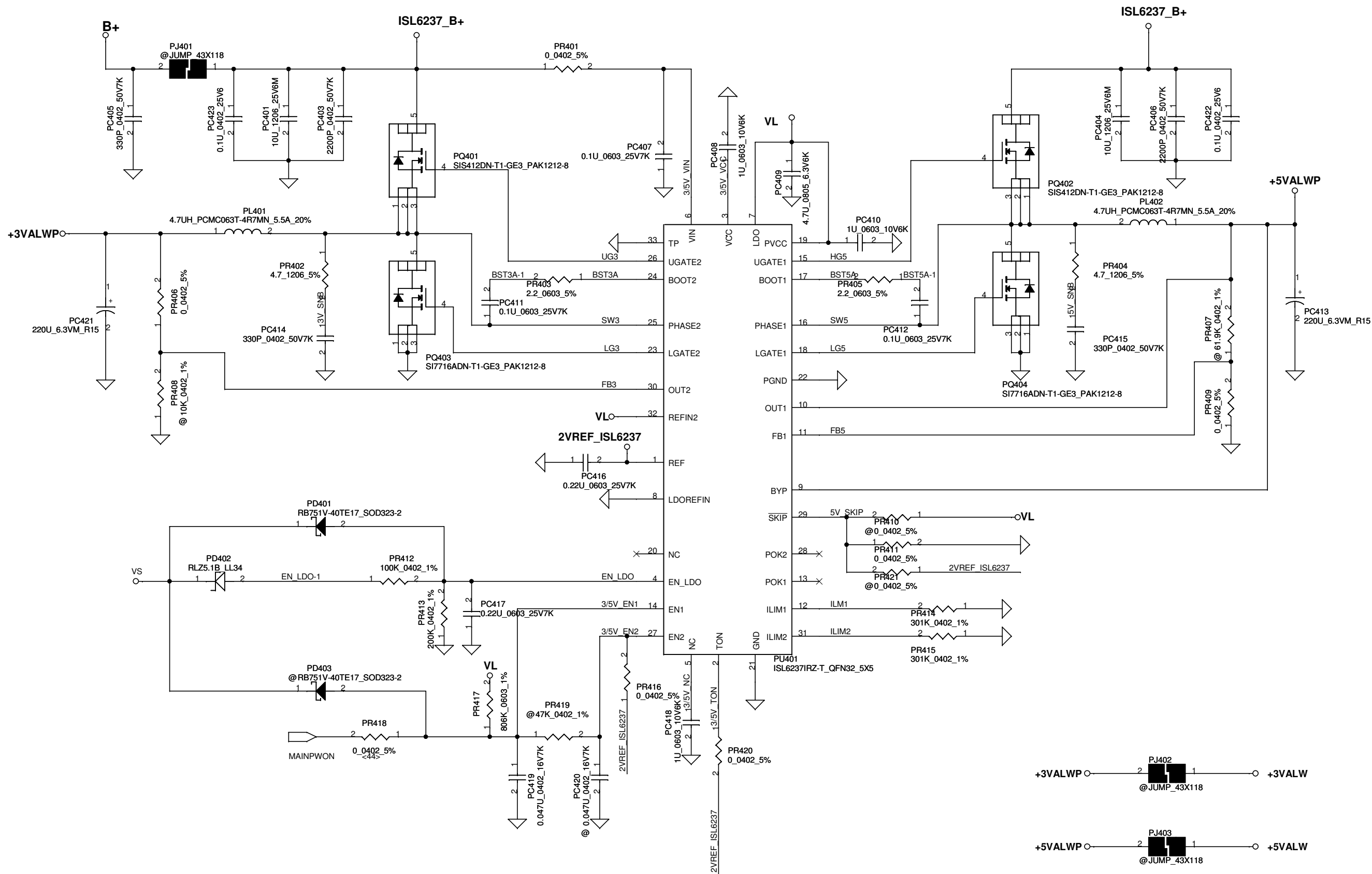
PH1 under CPU botten side :

CPU thermal protection at 92 degree C

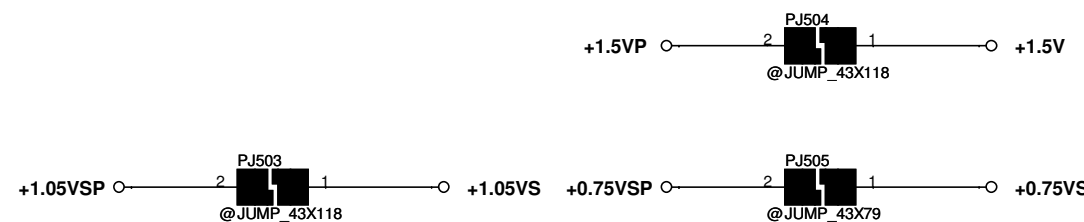
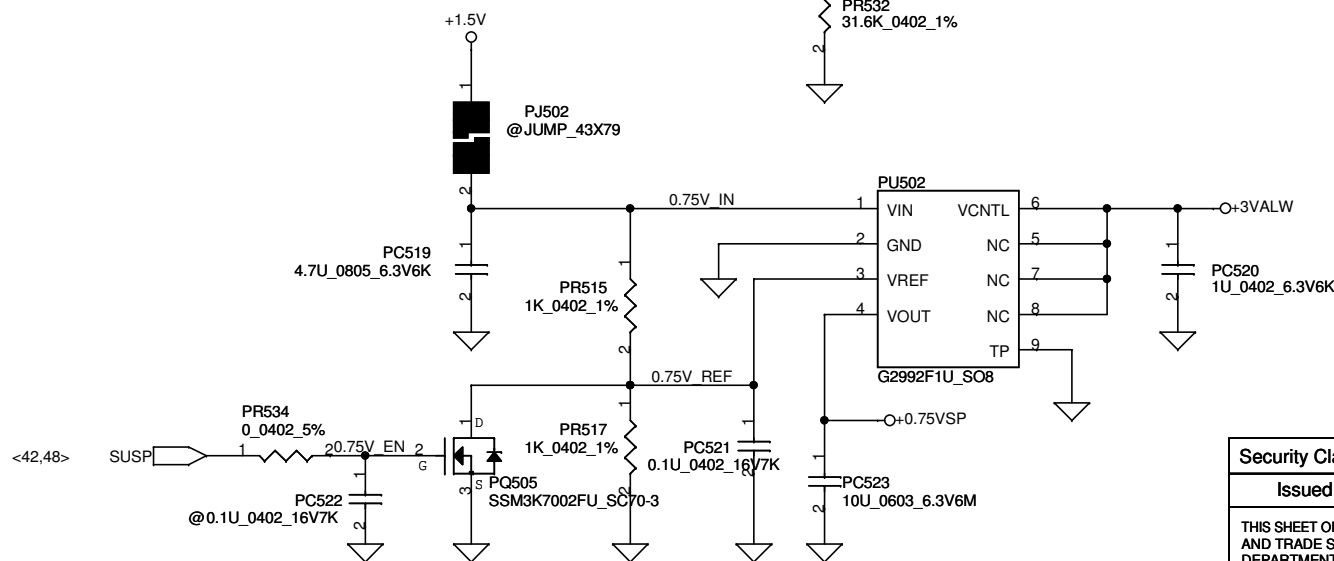
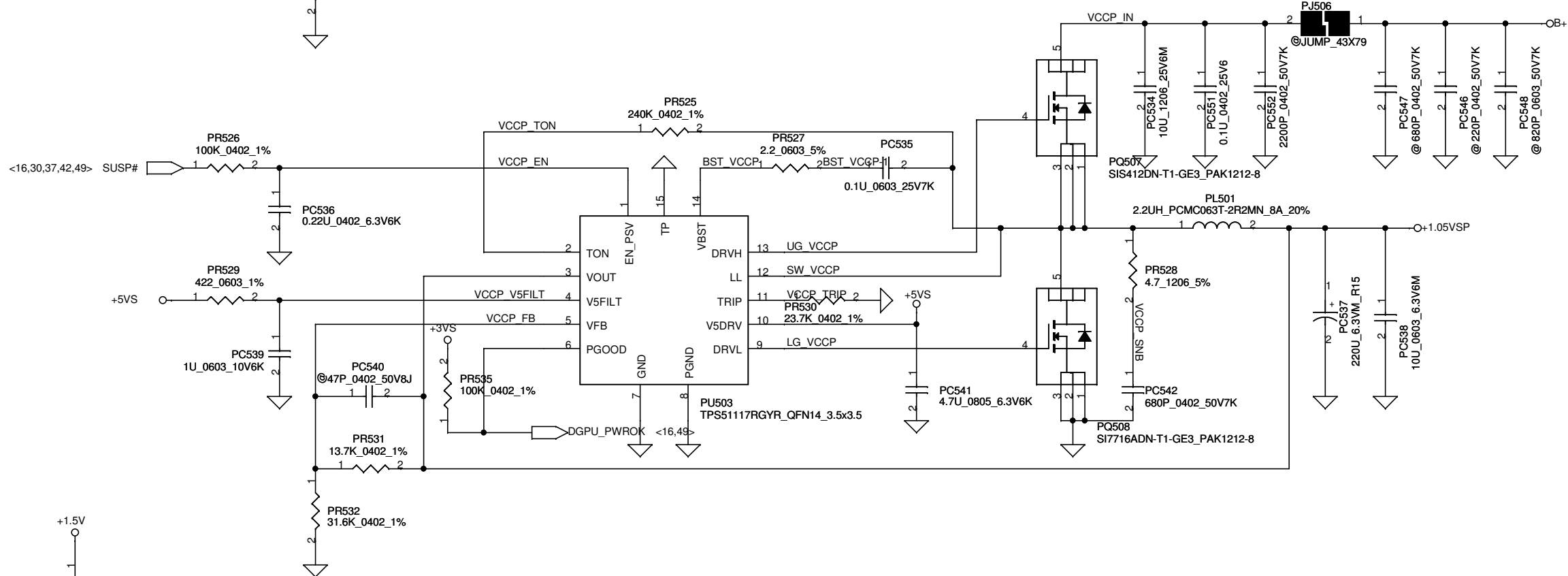
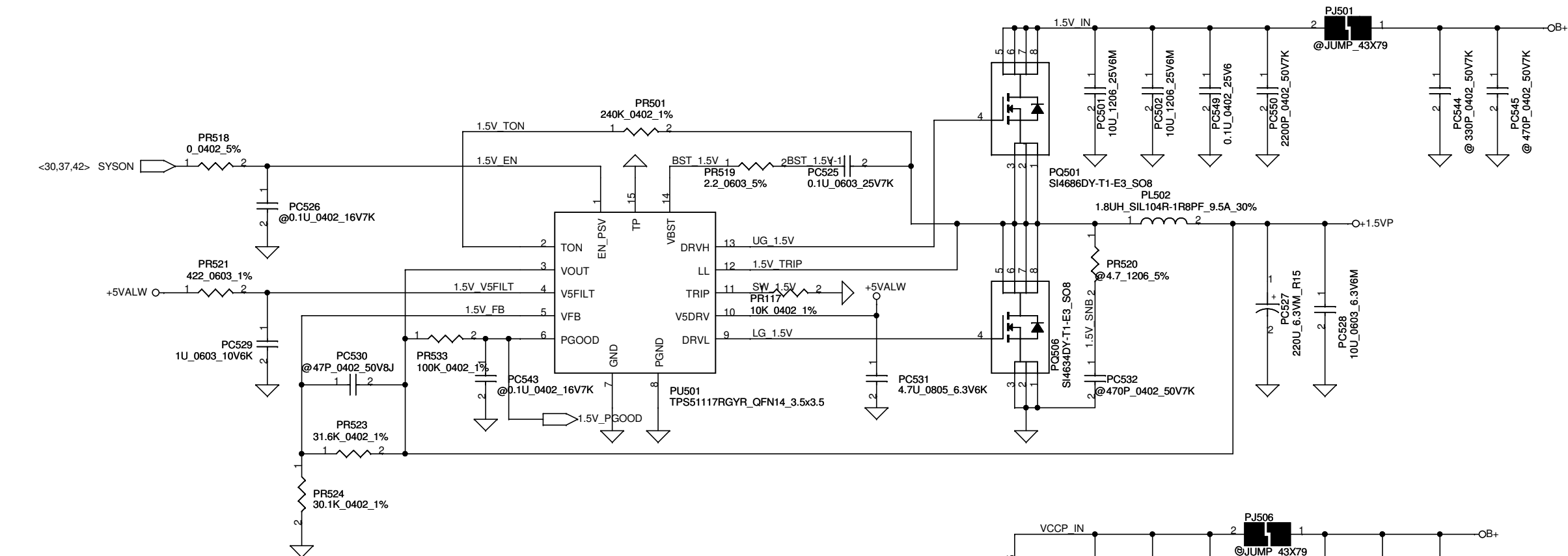
Recovery at 56 degree C



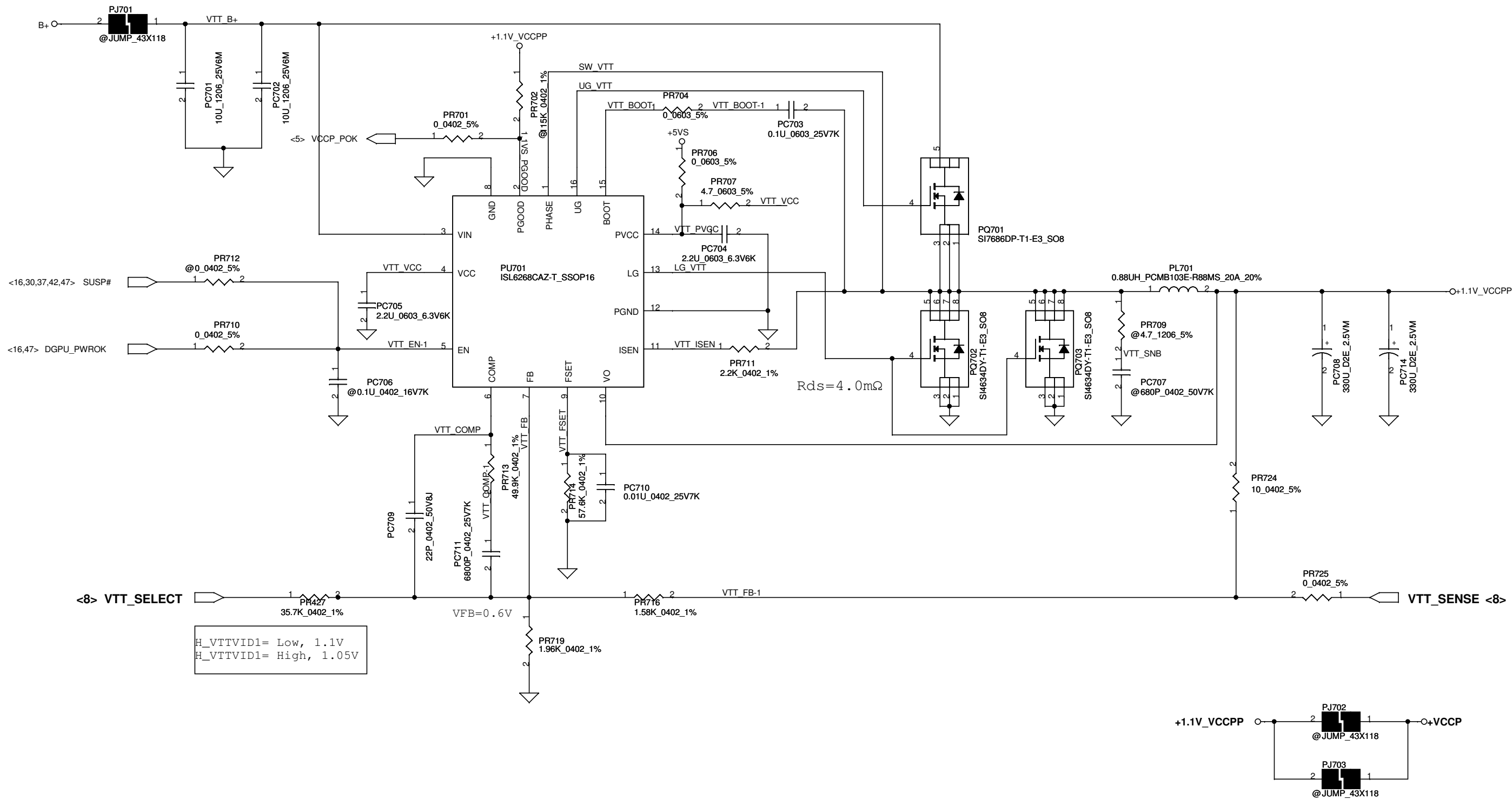
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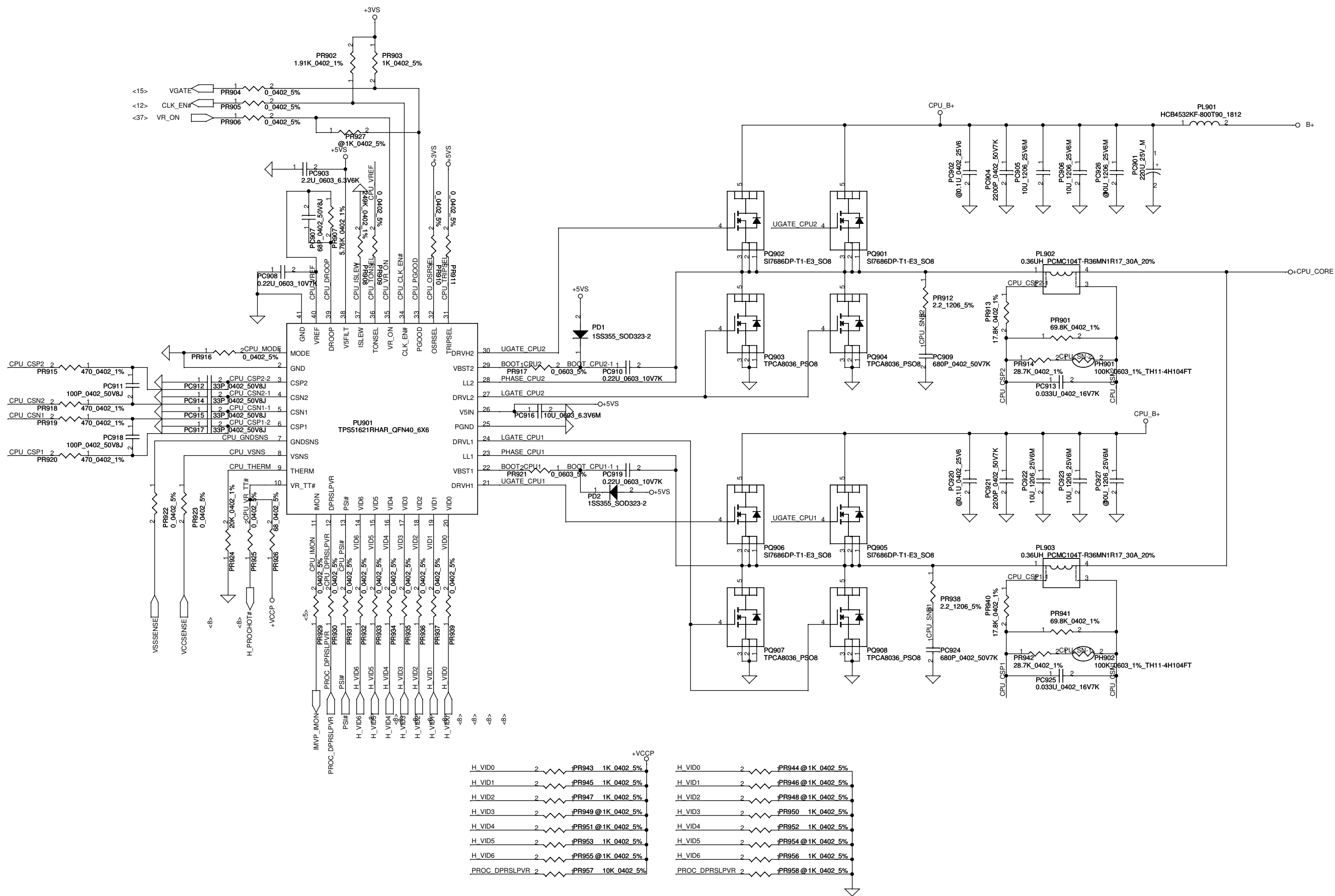
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Item	Reason for change	PG#	Modify List	Date	Phase
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2					
3					
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